7-Channel Configurable High Power PMIC

FEATURES

- **Four Monolithic Synchronous Buck DC/DCs (1A/1A/500mA/500mA)**
- **Buck DC/DCs Can Be Paralleled to Deliver Up to 2× Current with a Single Inductor**
- **Independent 1A Boost and 1A Buck-Boost DC/DCs**
- **Dual String I²C Controlled 40V LED Driver**
- **I²C Programmable Output Voltage, Operating Mode, and Switch Node Slew Rate for All DC/DCs**
- I²C Read Back of DC/DC, LED Driver, Fault Status
- I²C Slave Address Options: LTC3675 = 0001001X, LTC3675-1 = 0110100X
- Maskable Interrupts to Report DC/DC, V_{IN} and Die Temperature Faults
- Pushbutton ON/OFF/RESET
- Always-On 25mA LDO
- Low Quiescent Current: 16µA (All DC/DCs Off)
- 4mm × 7mm × 0.75mm 44-Lead QFN Package

APPLICATIONS

- High Power (5W to 10W) Single Cell Li-Ion/Polymer Applications
- Portable Industrial Applications, Handy Terminals, Portable Instruments
- Multioutput Low Voltage Power Supplies

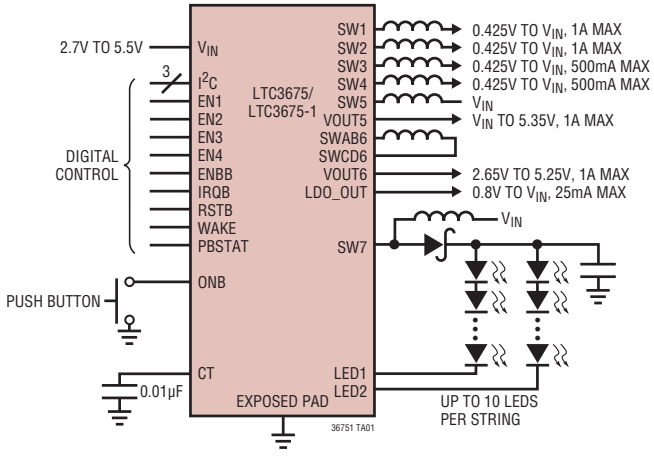
DESCRIPTION

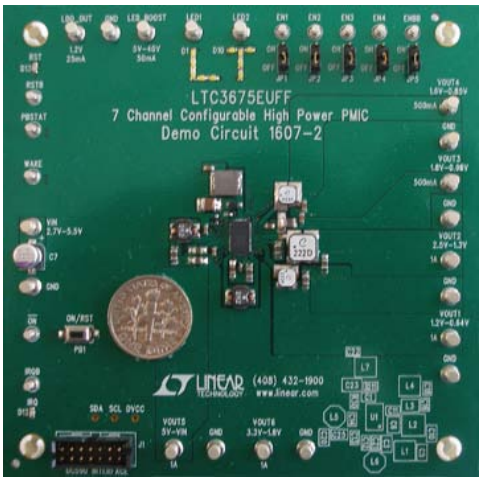
The LTC®3675/LTC3675-1 are a digitally programmable high efficiency multioutput power supplies plus dual string LED driver ICs optimized for high power single cell Li-Ion/Polymer applications. The DC/DCs consist of four synchronous buck converters (1A/1A/500mA/500mA), one synchronous boost DC/DC (1A), and one buck-boost DC/DC (1A) all powered from a 2.7V to 5.5V input. The 40V LED driver can regulate up to 25mA of current through two LED strings with up to 10 LEDs each. The LED driver may also be configured as a general purpose high voltage boost converter.

DC/DC enables, output voltages, switch slew rates and operating modes may all be independently programmed over I²C or used in standalone mode via simple I/O and power-up defaults. The buck DC/DCs may be used independently or paralleled to achieve higher output currents with a shared inductor. LED enable, 60dB brightness control and up/down gradation are programmed using I²C. Alarm levels for low V_{IN} and high die temperature may also be programmed via I²C with a maskable interrupt output to monitor DC/DC and system faults.

Pushbutton ON/OFF/RESET control and a power-on reset output provide flexible and reliable power-up sequencing. The LTC3675/LTC3675-1 are available in a low profile (0.75mm), thermally enhanced 44-lead 4mm × 7mm QFN package.

TYPICAL APPLICATION





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ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT5}, V_{OUT6}, FB1-6, LED_OV, EN1-4, ENBB, LED_FS, CT, WAKE, PBSTAT, IRQB, RSTB, ONB, DV_{CC}, SW5 ..... –0.3V to 6V (Static)

LDO_OUT, LDOFB ... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V

SCL, SDA ..... –0.3V to Lesser of (DV_{CC} + 0.3V) or 6V

SW1, SW2, SW3, SW4, SWAB6 ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V

SWCD6 ..... –0.3V to Lesser of (V_{OUT6} + 0.3V) or 6V

SW7 ..... –0.3V to 45V

I_{SW1}, I_{SW2} 1.4A

I_{SW3}, I_{SW4} 700mA

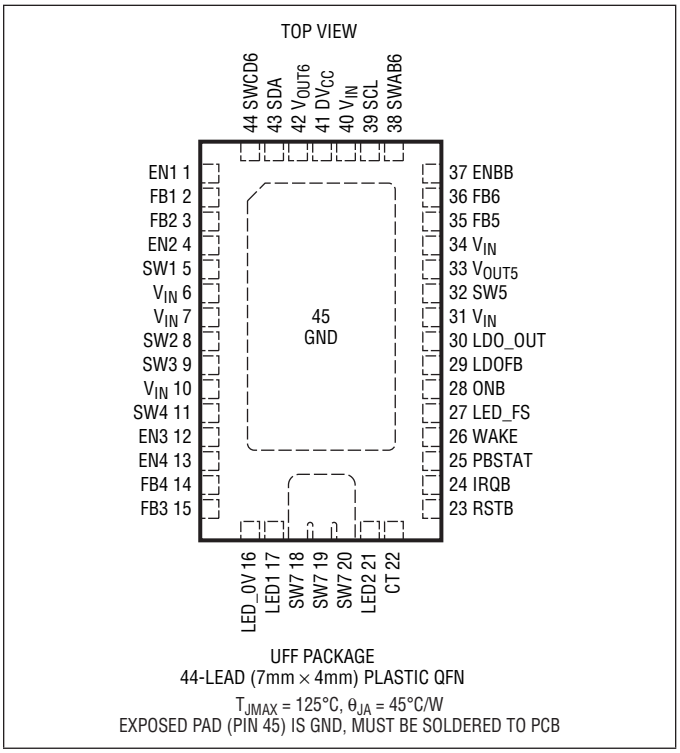
I_{SW5}, I_{SWAB6}, I_{SWCD6} 2.4A

I_{SW7} 2A

Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFF PACKAGE
44-LEAD (7mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 45°C/W

EXPOSED PAD (PIN 45) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3675EUFF#PBF	LTC3675EUFF#TRPBF	3675	44-Lead (7mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3675EUFF-1#PBF	LTC3675EUFF-1#TRPBF	36751	44-Lead (7mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Range		●	2.7		5.5	V
$V_{IN\_FALLING}$	Falling Undervoltage Threshold		●	2.35	2.45	2.55	V
V_{IN_RISING}	Rising Undervoltage Threshold		●	2.45	2.55	2.65	V
V_{IN_WARN}	Falling Undervoltage Warning Threshold	UV[2], UV[1], UV[0] = 000			2.7		V
		UV[2], UV[1], UV[0] = 001			2.8		V
		UV[2], UV[1], UV[0] = 010			2.9		V
		UV[2], UV[1], UV[0] = 011			3.0		V
		UV[2], UV[1], UV[0] = 100			3.1		V
		UV[2], UV[1], UV[0] = 101			3.2		V
		UV[2], UV[1], UV[0] = 110			3.3		V
		UV[2], UV[1], UV[0] = 111			3.4		V
V_{IN_HYS}	V_{IN} Undervoltage Warning Hysteresis				50		mV
$V_{IN\_WARN(LSB)}$	Undervoltage Warning Threshold Step Size		●	85	100	115	mV
OT	Overtemperature Shutdown				150		°C
OT_WARN	Overtemperature Warning Threshold; Die Temperature Below OT that Causes IRQB = 0	OT[1], OT[0] = 00 OT[1], OT[0] = 01 OT[1], OT[0] = 10 OT[1], OT[0] = 11			10 20 30 40		°C °C °C °C
I_{VIN_ALLOFF}	Input Supply Current	All Switching Regulators and LED Driver in Shutdown, ONB = HIGH; Sum of All V_{IN} Currents			16	28	µA
f_{OSC}	Voltage Regulator Switching Frequency	All Voltage Regulators	●	1.8	2.25	2.7	MHz
$V_{PGOOD(FALL)}$	Falling PGOOD Threshold Voltage	Full-Scale (1,1,1,1) Reference Voltage	●	88	92	96	%
$V_{PGOOD(HYS)}$	PGOOD Hysteresis	All Regulators Except LED Driver			1		%
1A Buck Regulator (Buck Regulators 1 and 2)							
$I_{VIN1,2}$	Pulse-Skipping Input Current Burst Mode® Operation Input Current	$V_{FB1} = V_{FB2}$ = 0.85V (Notes 4, 5) $V_{FB1} = V_{FB2}$ = 0.85V (Notes 4, 5)			105 20	200 50	µA µA
$I_{FWD1,2}$	PMOS Current Limit	(Note 6)		2.25	2.8	3.35	A
$V_{FB1,2(HIGH)}$	Feedback Regulation Voltage	Pulse-Skipping Mode Full-Scale (1,1,1,1)	●	780	800	820	mV
$V_{FB1,2(LOW)}$	Feedback Regulation Voltage	Pulse-Skipping Mode Full-Scale (0,0,0,0)	●	405	425	445	mV
$V_{LSB1,2}$	FB1, FB2 Regulation Voltage Step Size				25		mV
I_{FB12}	Feedback Leakage Current	$V_{FB1} = V_{FB2}$ = 0.85V		–50		50	nA
$D_{MAX1,2}$	Maximum Duty Cycle	$V_{FB1} = V_{FB2}$ = 0V	●	100			%
$R_{PMOS1,2}$	PMOS On-Resistance	$I_{SW1} = I_{SW2}$ = 100mA			265		mΩ
$R_{NMOS1,2}$	NMOS On-Resistance	$I_{SW1} = I_{SW2}$ = –100mA			280		mΩ
$I_{LEAKP1,2}$	PMOS Leakage Current	EN1 = EN2 = 0		–2		2	µA
$I_{LEAKN1,2}$	NMOS Leakage Current	EN1 = EN2 = 0		–2		2	µA
$R_{SWPD1,2}$	Output Pull-Down Resistance in Shutdown	EN1 = EN2 = 0 (I^2C Bit Set)			10		kΩ
$t_{SS1,2}$	Soft-Start Time				500		µs
500mA Buck Regulator (Buck Regulators 3 and 4)							
$I_{VIN3,4}$	Pulse-Skipping Input Current Burst Mode Operation Input Current	$V_{FB3} = V_{FB4}$ = 0.85V (Notes 4, 5) $V_{FB3} = V_{FB4}$ = 0.85V (Notes 4, 5)			105 20	200 50	µA µA
$I_{FWD3,4}$	PMOS Current Limit	(Note 6)		0.75	1.2	1.65	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FB3,4(HIGH)}$	Feedback Regulation Voltage	Pulse-Skipping Mode Full-Scale (1,1,1,1)	●	780	800	820	mV
$V_{FB3,4(LOW)}$	Feedback Regulation Voltage	Pulse-Skipping Mode Full-Scale (0,0,0,0)	●	405	425	445	mV
$V_{LSB3,4}$	FB3, FB4 Regulation Voltage Step Size				25		mV
$I_{FB3,4}$	Feedback Leakage Current	$V_{FB3} = V_{FB4}$ = 0.85V		–50		50	nA
$D_{MAX3,4}$	Maximum Duty Cycle	$V_{FB3} = V_{FB4}$ = 0V	●	100			%
$R_{PMOS3,4}$	PMOS On-Resistance	$I_{SW3} = I_{SW4}$ = 100mA			500		mΩ
$R_{NMOS3,4}$	NMOS On-Resistance	$I_{SW3} = I_{SW4}$ = –100mA			510		mΩ
$I_{LEAKP3,4}$	PMOS Leakage Current	EN3 = EN4 = 0		–1		1	µA
$I_{LEAKN3,4}$	NMOS Leakage Current	EN3 = EN4 = 0		–1		1	µA
$R_{SWPD3,4}$	Output Pull-Down Resistance in Shutdown	EN3 = EN4 = 0 (I^2C Bit Set)			10		kΩ
$t_{SS3,4}$	Soft-Start Time				500		µs
Buck Regulators Combined							
I_{FWD1+2}	PMOS Current Limit	FB2 = V_{IN} (Note 6)			5.6		A
I_{FWD2+3}	PMOS Current Limit	FB3 = V_{IN} (Note 6)			4		A
I_{FWD3+4}	PMOS Current Limit	FB4 = V_{IN} (Note 6)			2.4		A
1A Boost Regulator							
I_{VIN5}	PWM Mode Burst Mode Operation	V_{FB5} = 0.85V (Notes 4, 5) V_{FB5} = 0.85V (Notes 4, 5)			150 35	300 60	µA µA
$V_{OUT5(MAX)}$	Maximum Regulated Output Voltage			5.35	5.55	5.75	V
I_{FWD5}	Forward Current Limit	(Note 6)		2.5	3.15	3.9	A
$V_{FB5(HIGH)}$	Feedback Regulation Voltage	PWM Mode Full-Scale (1,1,1,1)	●	780	800	820	mV
$V_{FB5(LOW)}$	Feedback Regulation Voltage	PWM Mode Full-Scale (0,0,0,0)	●	405	425	445	mV
V_{LSB5}	FB5 Regulation Voltage Step Size				25		mV
I_{FB5}	Feedback Leakage Current	V_{FB5} = 0.85V		–50		50	nA
DC_{MAX5}	Maximum Duty Cycle	NMOS Switch			90		%
R_{PMOS5}	PMOS On-Resistance				260		mΩ
R_{NMOS5}	NMOS On-Resistance				275		mΩ
I_{LEAKP}	PMOS Switch Leakage Current			–2		2	µA
I_{LEAKN}	NMOS Switch Leakage Current			–2		2	µA
R_{OUTPD5}	Output Pull-Down Resistance in Shutdown	Boost Regulator Off			10		kΩ
t_{SS5}	Soft-Start Time				500		µs
1A Buck-Boost Regulator							
I_{VIN6}	PWM Mode Burst Mode Operation	V_{FB6} = 0.85V (Note 4, 5) V_{FB6} = 0.85V(Note 4, 5)			220 20	400 40	µA µA
$V_{OUT6(LOW)}$	Minimum Regulated Output Voltage				2.65	2.8	V
$V_{OUT6(HIGH)}$	Maximum Regulated Output Voltage			5.25	5.65		V
I_{FWD6}	Forward Current Limit	PWM Mode (Note 6)		2.1	2.65	3.2	A
I_{PEAK6}	Peak Current Limit	Burst Mode Operation (Note 6)		200	275	350	mA
I_{ZERO6}	Zero Current Limit	Burst Mode Operation		–30	0	30	mA
$V_{FB6(HIGH)}$	Feedback Regulation Voltage	PWM Mode Full-Scale (1,1,1,1)	●	780	800	820	mV
$V_{FB6(LOW)}$	Feedback Regulation Voltage	PWM Mode Full-Scale (0,0,0,0)	●	405	425	445	mV
V_{LSB6}	FB6 Regulation Voltage Step Size				25		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB6}	Feedback Leakage Current	V_{FB6} = 0.85V		–50		50	nA
$DC6_{BUCK(MAX)}$	Maximum Buck Duty Cycle	Duty Cycle of PMOS Switch A	●	100			%
$DC6_{BOOST(MAX)}$	Maximum Boost Duty Cycle	Duty Cycle of NMOS Switch C			75		%
R_{PMOS6}	PMOS On-Resistance	Switches A and D			260		mΩ
R_{NMOS6}	NMOS On-Resistance	Switches B and C			275		mΩ
I_{LEAKP}	PMOS Switch Leakage Current			–2		2	µA
I_{LEAKN}	NMOS Switch Leakage Current			–2		2	µA
t_{SS}	Soft-Start Time				500		µs
R_{OUTPD6}	Output Pull-Down Resistance in Shutdown	ENBB = 0			10		kΩ
LED Driver; R_{LED_FS} = 20kΩ							
I_{VIN7}	Input Current (MODE0 = MODE1 = 0)	LED_OV = 0.85V (Notes 4, 5)			700	1000	µA
V_{LED_OV}	LED Overvoltage Threshold Feedback Voltage	Operating in LED Mode Operating in Boost Mode	● ●	805 770	825 800	845 830	mV mV
V_{LED_FS}	LED Full-Scale Voltage		●	775	800	825	mV
$V_{LED1,2}$	LED Pin Regulation Voltage	(Note 7)			300		mV
$V_{LED1,2\_CLMP}$	LED Regulation Voltage Clamp		●	6.0		8.3	V
I_{LIM7}	Maximum Current Limit	(Note 6)		1.6	1.85	2.15	A
I_{LED_FS}	LED Full-Scale Current		●	23.25	25.0	26.75	mA
I_{LED_2FS}	LED Full Current High Current Mode		●	46.5	50	53.5	mA
I_{LED_MATCH}	LED1 and LED2 Current Matching at Full-Scale	$\frac{\lvert I_{LED1} - I_{LED2} \rvert}{\left(\frac{I_{LED1} + I_{LED2}}{2}\right)} \bullet 100$	●			1	%
I_{LED_LSB}	LED Current LSB				98		µA
R_{NMOS7}	NMOS On-Resistance				300		mΩ
I_{LEAK_NMOS7}	NMOS Switch Leakage	V_{SW7} = 5.5V		–1		1	µA
F_{LEDOSC}	Oscillator Frequency		●	450	562.5	675	kHz
DC_{MAX7}	Maximum Duty Cycle	NMOS Switch			97		%
25mA Always-On LDO							
V_{LDOFB}	Feedback Regulation Voltage		●	780	800	820	mV
R_{DO}	Dropout Resistance				12		Ω
I^2C Port							
DV_{CC}	Input Supply Voltage		●	1.6		5.5	V
I_{DVCC}	Input Supply Current	SCL/SDA= 0kHz			0.3	1	µA
DV_{CC_UVLO}	DV_{CC} UVLO				1		V
ADDRESS	I^2C Address	LTC3675 LTC3675-1	● ●		0001001[R/WB] 0110100[R/WB]		
V_{IH}	Input High Voltage	SDA/SCL			70		$\%DV_{CC}$
V_{IL}	Input Low Voltage	SDA/SCL			30		$\%DV_{CC}$
I_{IH}	Input High Current	SDA/SCL		–1	0	1	µA
I_{IL}	Input Low Current	SDA/SCL		–1	0	1	µA
V_{OL_SDA}	SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_SDA}	Hold Time After Repeated Start Condition			0.6			µs
t_{SU_STA}	Repeated Start Condition Set-Up Time			0.6			µs
t_{SU_STO}	Stop Condition Set-Up Time			0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output			0		900	ns
$t_{HD\_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Clock/Data Fall Time	C_B = Capacitance of One Bus Line (pF)		20+0.1C_B		300	ns
t_r	Clock/Data Rise Time	C_B = Capacitance of One Bus Line (pF)		20+0.1C_B		300	ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
Interface Logic Pins (PBSTAT, WAKE, RSTB, IRQB, ONB)							
$I_{LK(HIGH)}$	Output High Leakage Current	3.6V at Pin		–1		1	µA
V_{OL}	Output Low Voltage	3mA into Pin			100	400	mV
$V_{ONB(HIGH)}$	ONB High Threshold				800	1200	mV
$V_{ONB(LOW)}$	ONB Low Threshold			400	700		mV
Interface Logic Pins (EN1, EN2, EN3, EN4, ENBB)							
V_{HI_ALLOFF}	Enable Rising Threshold	All Regulators and LED Driver Disabled	●	400	650	1200	mV
V_{EN_HYS}	Enable Falling Hysteresis				60		mV
V_{HI}	Enable Rising Threshold	At Least One Regulator/LED Driver Enabled	●	380	400	420	mV
I_{EN}	Enable Pin Leakage Current	EN = 3.6V		–1		1	µA
Pushbutton Parameters; CT = 0.01µF							
t_{ONB_LO}	ONB Low Time to PBSTAT Low	WAKE High		28	50	72	ms
t_{ONB_WAKE}	ONB Low Time to WAKE High			280	400	520	ms
t_{ONB_HR}	ONB Low to Hard Reset			3.5	5	6.5	sec
t_{HR}	Time for Which All Enabled Regulators are Disabled			0.7	1	1.3	sec
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width			28	50	72	ms
t_{WAKE_ON}	WAKE High Time			3.5	5	6.5	sec

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3675/LTC3675-1 are tested under pulsed load conditions such that $T_A \approx T_J$. The LTC3675/LTC3675-1 are guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LTC3675/LTC3675-1 include overtemperature protection which protects the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Static current, switches not switching. Actual current may be higher due to gate charge losses at the switching frequency.

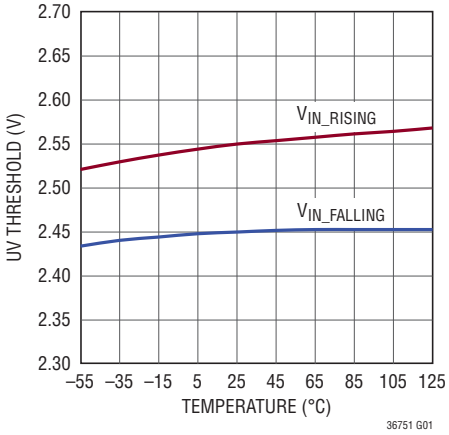
Note 5: Currents measured at a specific V_{IN} pin. Buck 1 (V_{IN}, Pin 6); Buck 2 (V_{IN}, Pin 7); Buck 3 and Buck 4 (V_{IN}, Pin 10); Boost and Buck Boost (V_{IN}, Pin 34); LED driver (V_{IN}, Pin 31).

Note 6: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation over time.

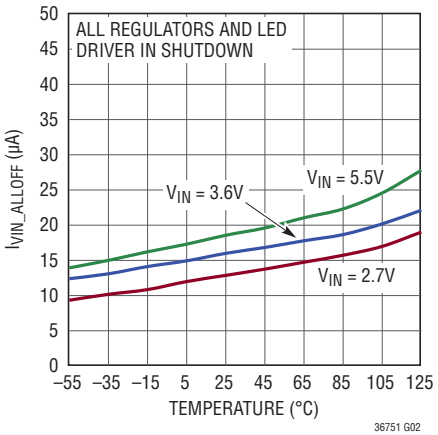
Note 7: With dual string operation, the LED pin with the lower voltage sets the regulation point.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

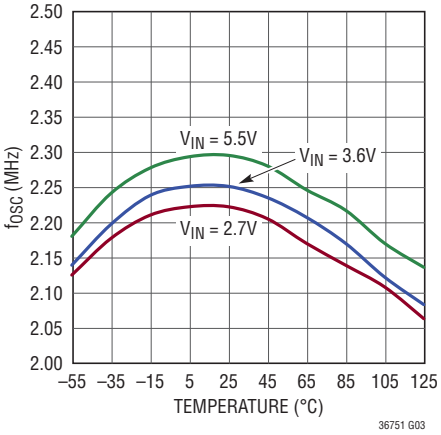
Undervoltage Threshold vs Temperature



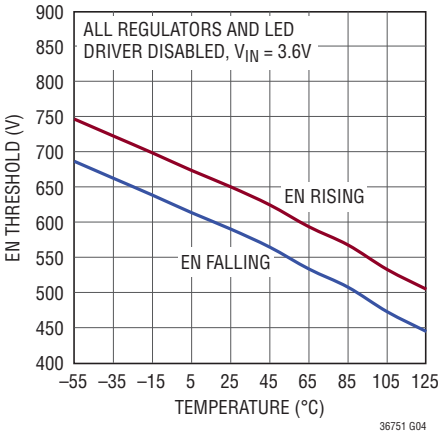
Input Supply Current vs Temperature



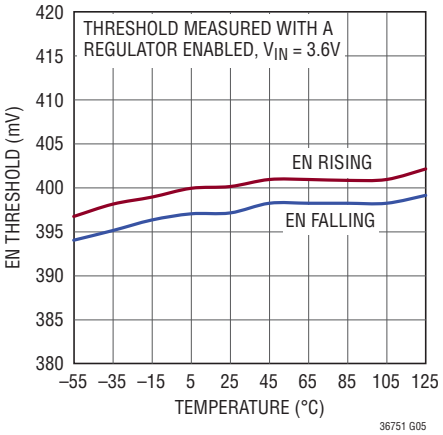
Oscillator Frequency vs Temperature



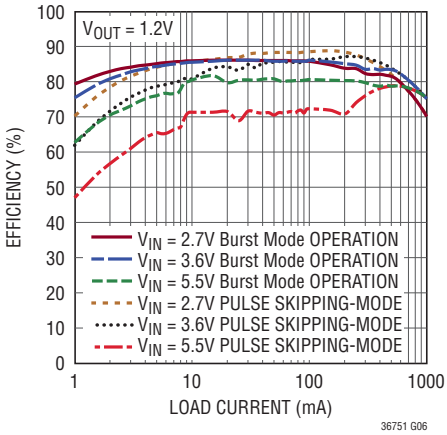
Enable Threshold vs Temperature



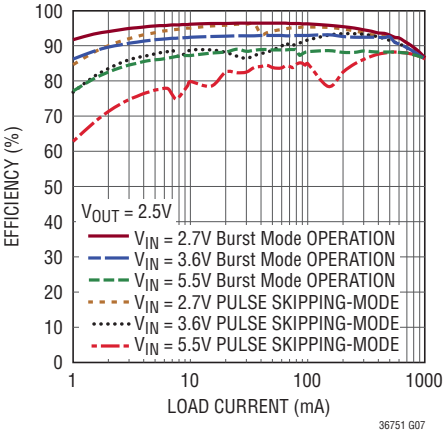
Enable Pin Precision Threshold vs Temperature



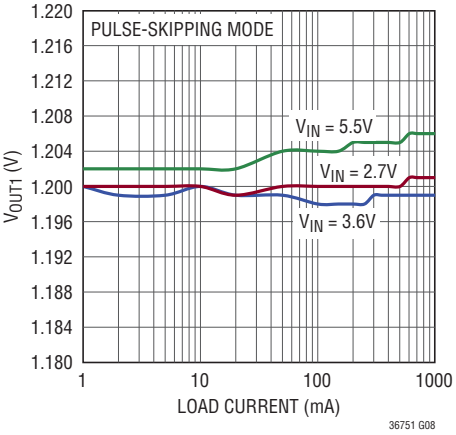
1A Buck Regulators, Efficiency vs Load



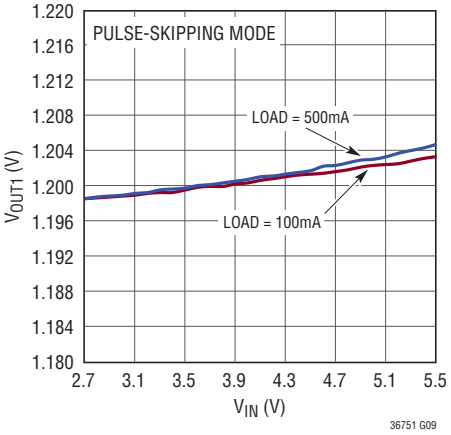
1A Buck Regulators, Efficiency vs Load



1A Buck Regulators, Load Regulation

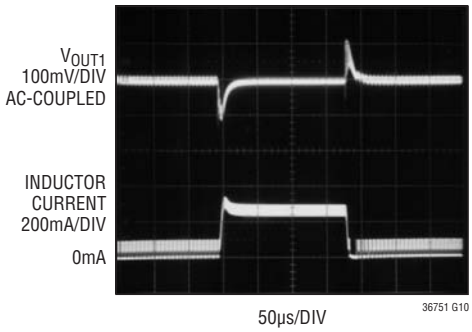


1A Buck Regulators, Line Regulation



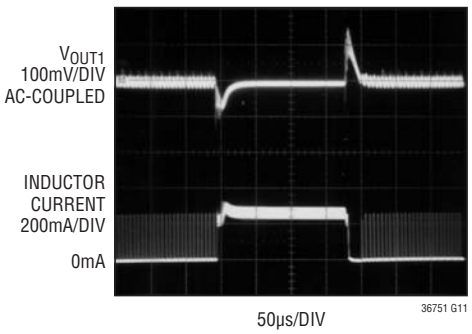
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

1A Buck Regulators, Transient Response (Pulse-Skipping Mode)



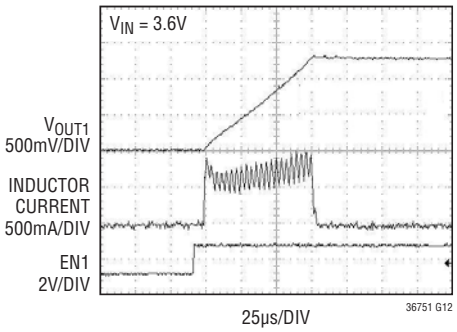
LOAD STEP = 100mA TO 700mA
V_{IN} = 3.6V, V_{OUT1} = 1.2V

1A Buck Regulators, Transient Response (Burst Mode Operation)

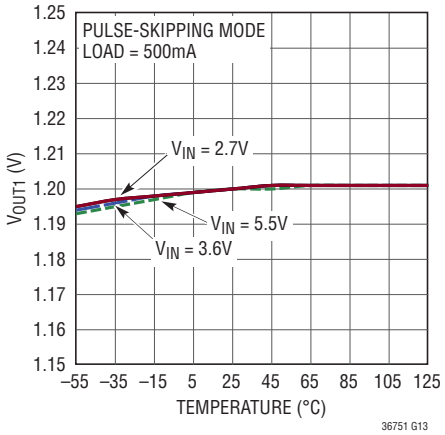


LOAD STEP = 100mA TO 700mA
V_{IN} = 3.6V, V_{OUT1} = 1.2V

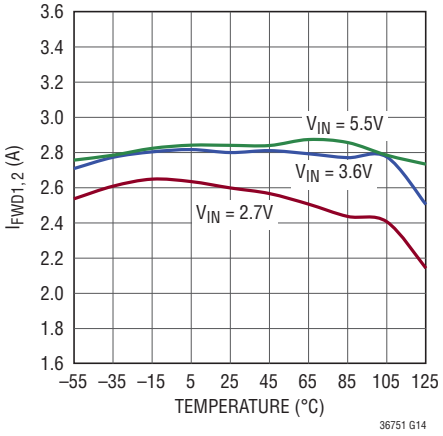
1A Buck Regulators, No Load Start-Up Transient (Pulse-Skipping Mode)



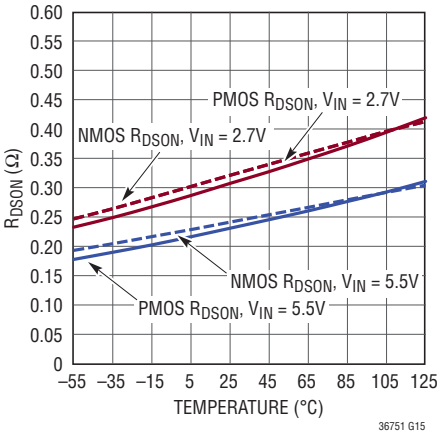
1A Buck Regulators, V_{OUT1} vs Temperature



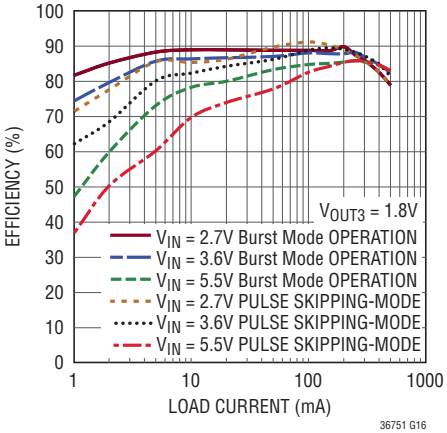
1A Buck Regulators, PMOS Current Limit vs Temperature



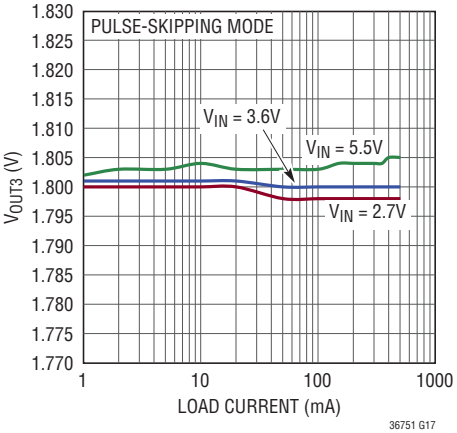
1A Buck Regulators, Switch R_{DSON} vs Temperature



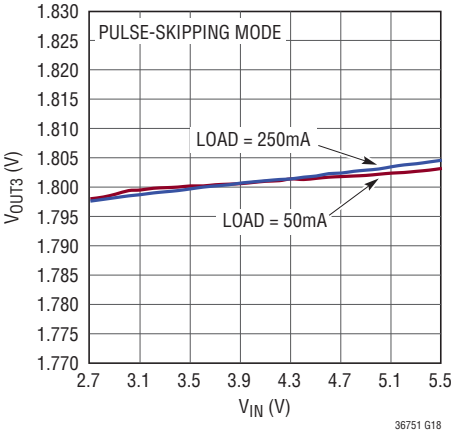
500mA Buck Regulators, Efficiency vs Load



500mA Buck Regulators, Load Regulation

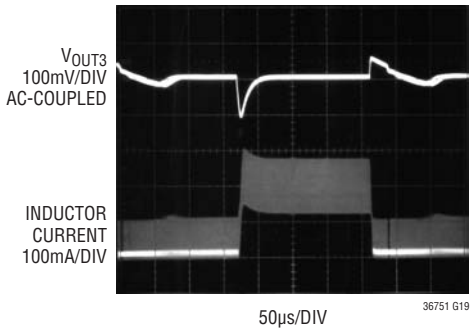


500mA Buck Regulators, Line Regulation



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

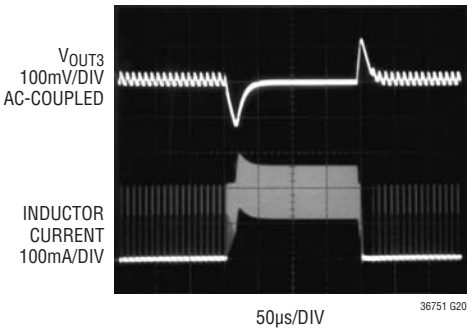
500mA Buck Regulators Transient Response (Pulse-Skipping Mode)



50µs/DIV

LOAD STEP = 50mA to 300mA
V_{IN} = 3.6V, V_{OUT3} = 1.8V

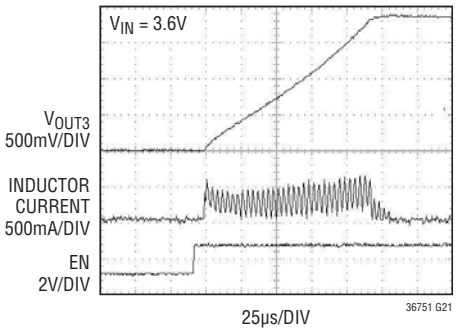
500mA Buck Regulators Transient Response (Burst Mode Operation)



50µs/DIV

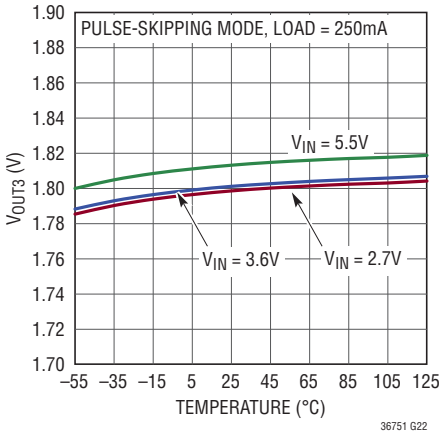
LOAD STEP = 50mA to 300mA
V_{IN} = 3.6V, V_{OUT3} = 1.8V

500mA Buck Regulators No Load Start-Up Transient (Pulse-Skipping Mode)

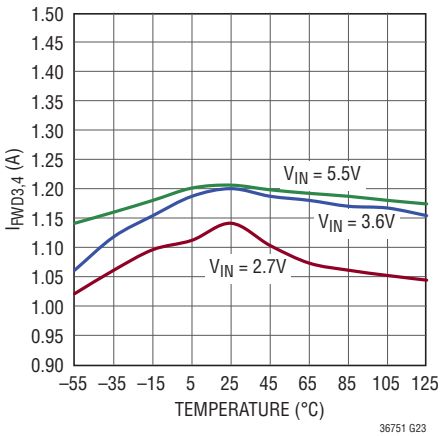


25µs/DIV

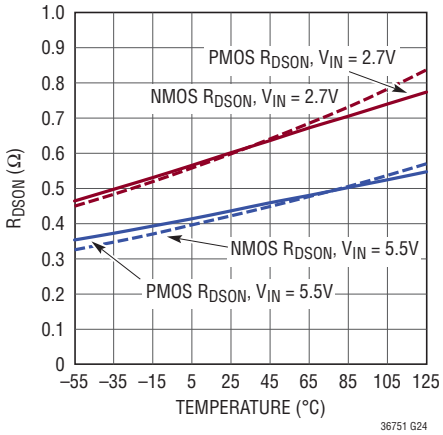
500mA Buck Regulators, V_{OUT3} vs Temperature



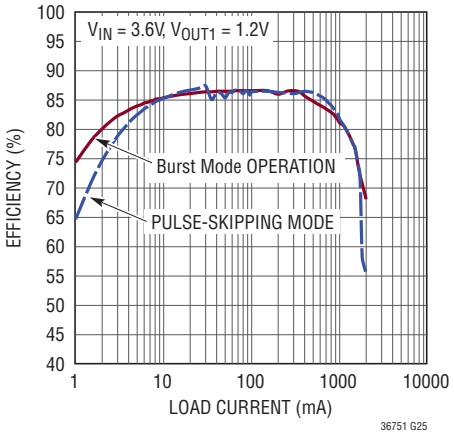
500mA Buck Regulators, PMOS Current Limit vs Temperature



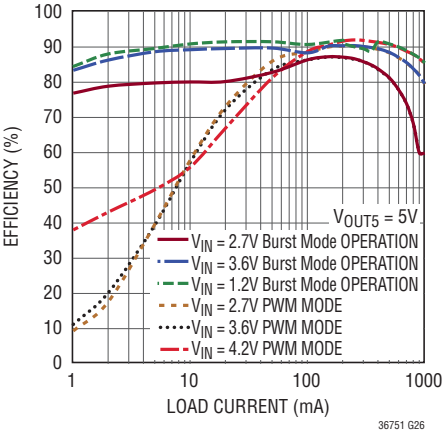
500mA Buck Regulators, Switch R_{DSON} vs Temperature



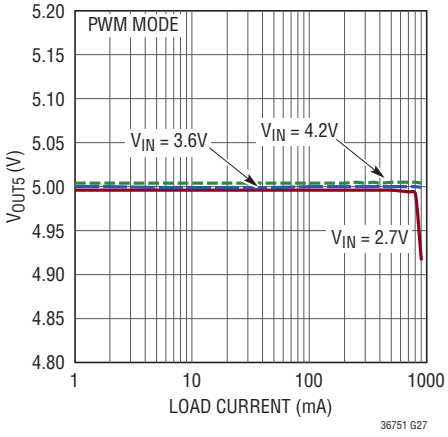
Ganged Buck Regulators 1 and 2, Efficiency vs Load



Boost Regulator, Efficiency vs Load

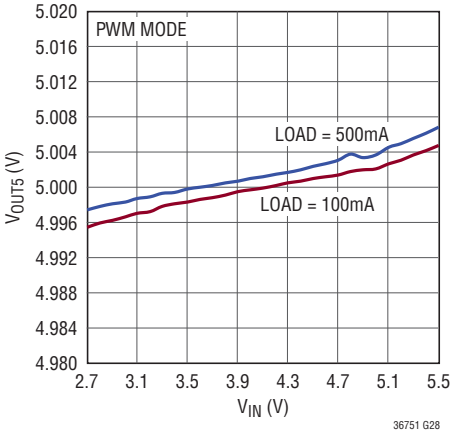


Boost Regulator, Load Regulation

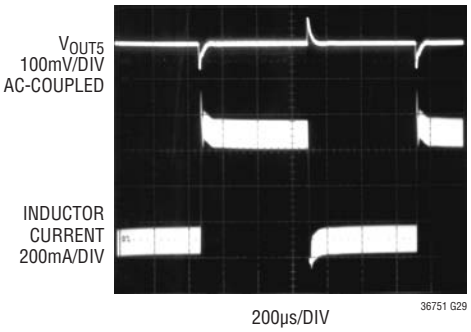


TYPICAL PERFORMANCE CHARACTERISTICS

Boost Regulator, Line Regulation



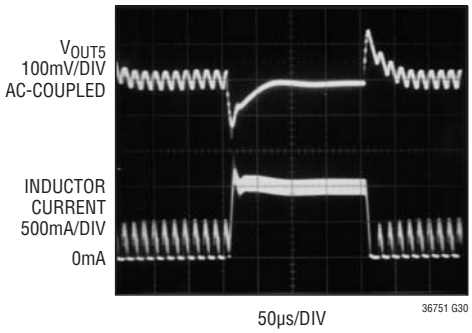
Boost Regulator Transient Response (PWM Mode)



200µs/DIV

LOAD STEP = 100mA to 600mA
V_{IN} = 3.6V, V_{OUT5} = 5V

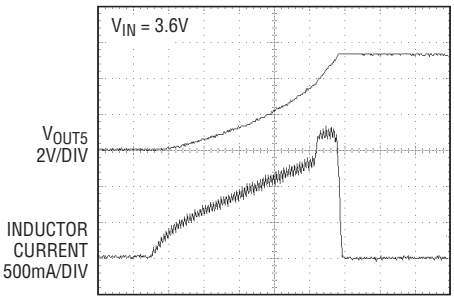
Boost Regulator Transient Response (Burst Mode Operation)



50µs/DIV

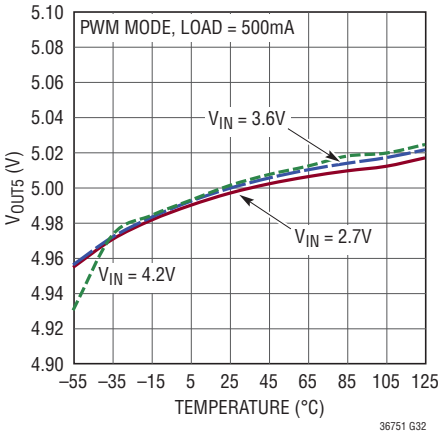
LOAD STEP = 100mA to 600mA
V_{IN} = 3.6V, V_{OUT5} = 5V

Boost Regulator, No Load Start-Up Transient, PWM Mode

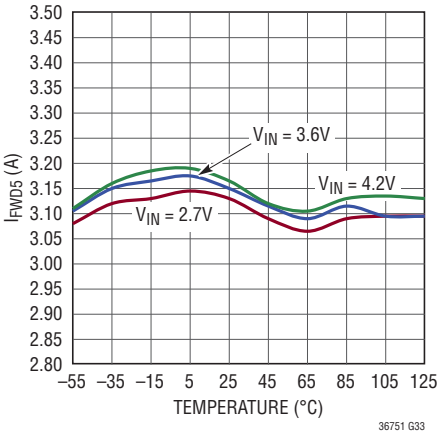


50µs/DIV

Boost Regulator, V_{OUT5} vs Temperature

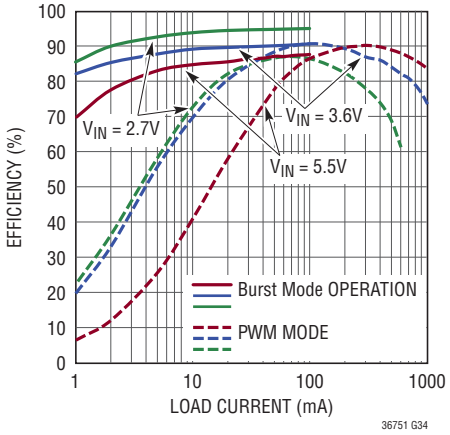


Boost Regulator, Forward Current Limit vs Temperature

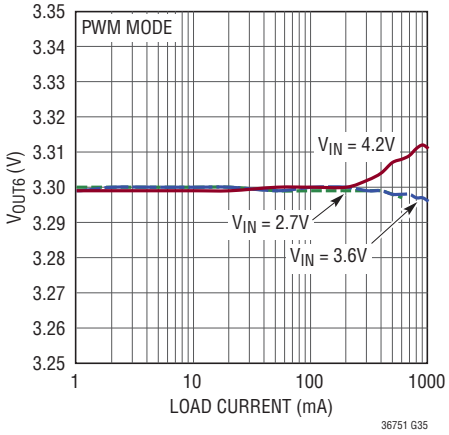


TYPICAL PERFORMANCE CHARACTERISTICS

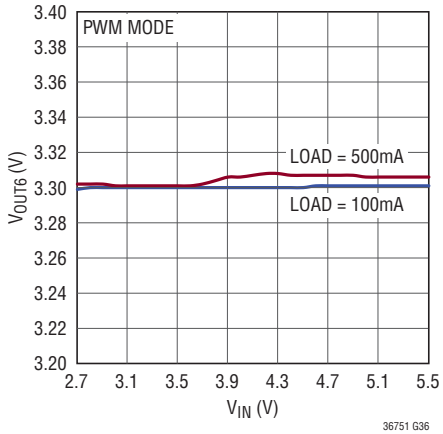
Buck-Boost Regulator, Efficiency vs Load



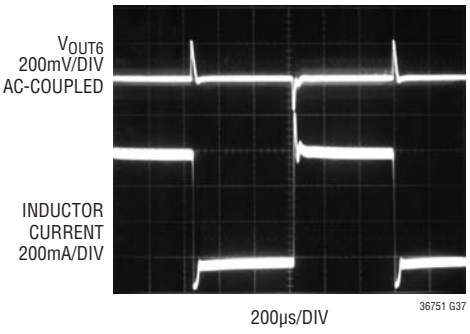
Buck-Boost Regulator, Load Regulation



Buck-Boost Regulator, Line Regulation



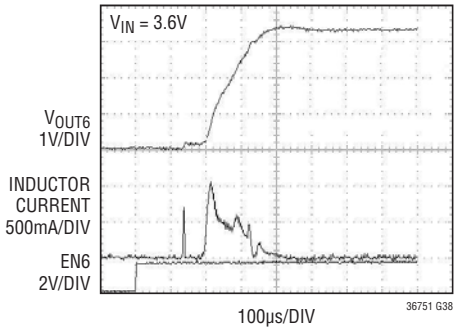
Buck-Boost Regulator Transient Response (PWM Mode)



200µs/DIV

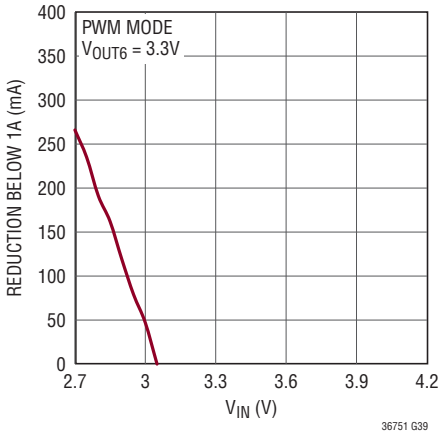
LOAD STEP = 100mA to 600mA
V_{IN} = 3.6V, V_{OUT6} = 3.3V

Buck-Boost Regulator No Load Start-Up (PWM Mode)



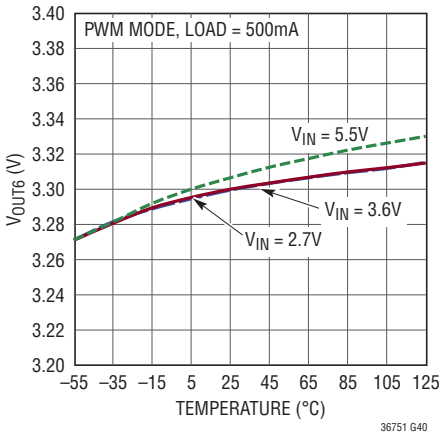
100µs/DIV

Buck-Boost Regulator, Reduction in Load Current Deliverability

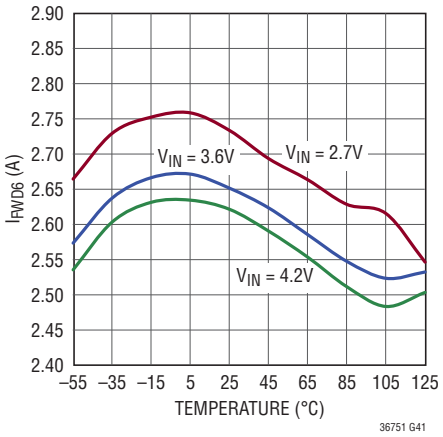


TYPICAL PERFORMANCE CHARACTERISTICS

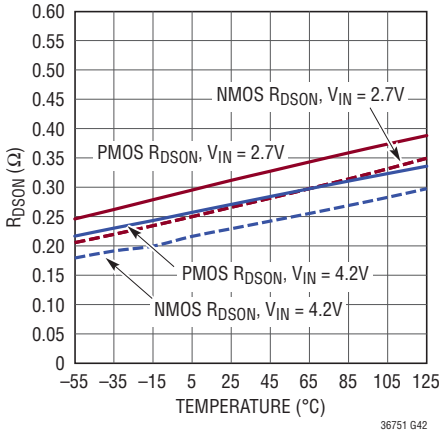
Buck-Boost Regulator, V_{OUT6} vs Temperature



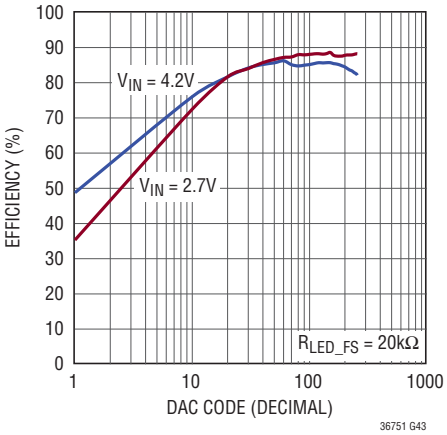
Buck-Boost Regulator, Forward Current Limit vs Temperature



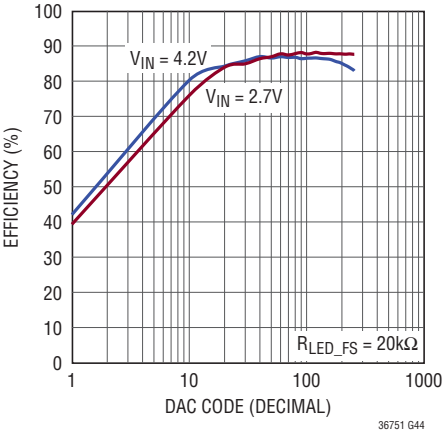
Buck-Boost Regulator, Switch R_{DSON} vs Temperature



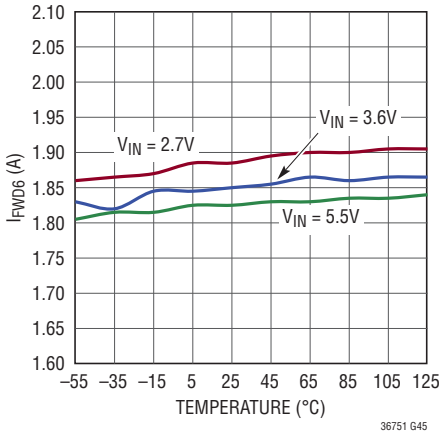
LED Driver, Dual String Efficiency, 10 LEDs per String



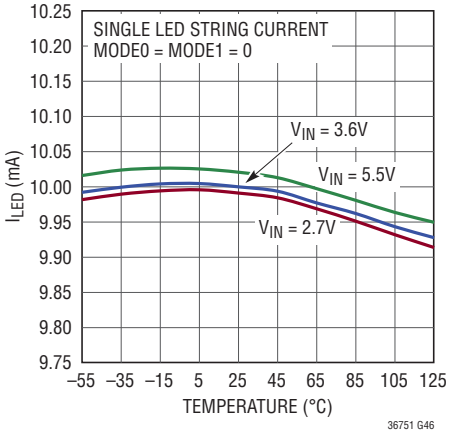
LED Driver, Dual String Efficiency, 4 LEDs per String



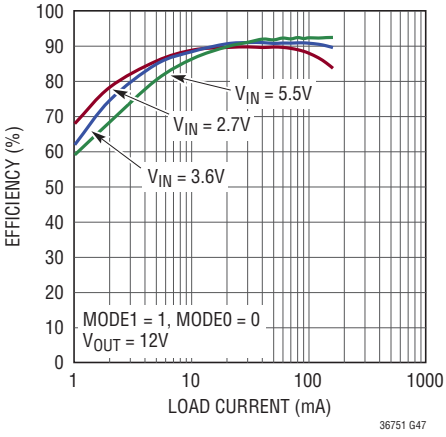
LED Driver, Forward Current Limit vs Temperature



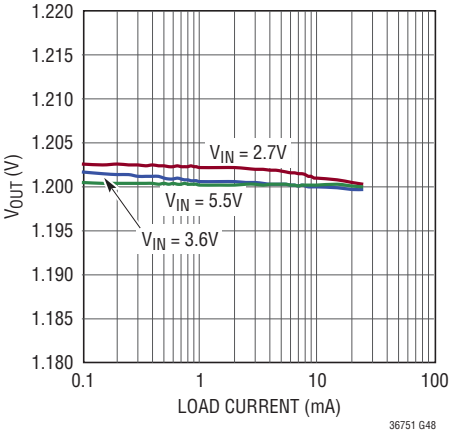
LED Driver, LED Current vs Temperature



High Voltage Boost Regulator, Efficiency vs Load



Always-On LDO, Load Regulation



PIN FUNCTIONS

EN1 (Pin 1): Buck Regulator 1 Enable Input. Active high. This pin is a high impedance input; do not float.

FB1 (Pin 2): Buck Regulator 1 Feedback Pin. Receives feedback by a resistor divider connected across the output.

FB2 (Pin 3): Buck Regulator 2 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB2 to V_{IN} combines buck regulator 2 with buck regulator 1 for higher current.

EN2 (Pin 4): Buck Regulator 2 Enable Input. Active high. This pin is a high impedance input; do not float.

SW1 (Pin 5): Buck Regulator 1 Switch Node. External inductor connects to this pin.

V_{IN} (Pin 6): Buck Regulator 1 Input Supply. A 10µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 7, 10, 31, 34, 40).

V_{IN} (Pin 7): Buck Regulator 2 Input Supply. A 10µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 6, 10, 31, 34, 40).

SW2 (Pin 8): Buck Regulator 2 Switch Node. External inductor connects to this pin.

SW3 (Pin 9): Buck Regulator 3 Switch Node. External inductor connects to this pin.

V_{IN} (Pin 10): Buck Regulators 3 and 4 Input Supply. A 10µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 6, 7, 31, 34, 40).

SW4 (Pin 11): Buck Regulator 4 Switch Node. External inductor connects to this pin.

EN3 (Pin 12): Buck Regulator 3 Enable Input. Active high. This pin is a high impedance input; do not float.

EN4 (Pin 13): Buck Regulator 4 Enable Input. Active high. This pin is a high impedance input; do not float.

FB4 (Pin 14): Buck Regulator 4 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB4 to V_{IN} combines buck regulator 4 with buck regulator 3 for higher current.

FB3 (Pin 15): Buck Regulator 3 Feedback Pin. Receives feedback by a resistor divider connected across the output. Connecting FB3 to V_{IN} combines buck regulator 3 with buck regulator 2 for higher current.

LED_OV (Pin 16): Overvoltage Protection Pin for LED Driver.

LED1 (Pin 17): Connect a string of up to 10 LEDs to this pin.

SW7 (Pins 18, 19, 20): LED Driver Switch Node. External inductor connects to these pins.

LED2 (Pin 21): Connect a string of up to 10 LEDs to this pin.

CT (Pin 22): Timing Capacitor Pin. A capacitor connected to GND sets a time constant which is scaled for use by the WAKE, RSTB and IRQB pins.

RSTB (Pin 23): Reset Pin. Open drain output. When the regulated output voltage of any enabled switching regulator is more than 8% below its programmed level, this pin is driven LOW. Assertion delay is scaled by the C_T capacitor.

IRQB (Pin 24): Interrupt Pin. Open drain output. When undervoltage, overtemperature, or an unmasked error condition is detected, this pin is driven LOW.

PBSTAT (Pin 25): Pushbutton Status Pin. Open drain output. This pin provides a debounced and glitch free status of the ONB pin.

PIN FUNCTIONS

WAKE (Pin 26): Open Drain Output. When the ONB pin is pressed and released, the signal is debounced and the WAKE signal is held HIGH for a minimum time period that is scaled by the C_T capacitor.

LED_FS (Pin 27): A resistor connected from this pin to GND programs full-scale LED current.

ONB (Pin 28): Pushbutton Input. Active low.

LDOFB (Pin 29): LDO Feedback Pin. A resistor divider from LDO_OUT to GND provides feedback.

LDO_OUT (Pin 30): Output of Always-On LDO. Decouple with a 10µF capacitor to GND.

V_{IN} (Pin 31): Quiet Input Supply Used to Power Non-Switching Control Circuitry. A 2.2µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 6, 7, 10, 34, 40).

SW5 (Pin 32): Boost Regulator Switch Node. External inductor connects to this pin.

V_{OUT5} (Pin 33): Boost Regulator Output. Connect two 22µF capacitors to GND.

V_{IN} (Pin 34): Quiet Input Supply Used to Power Non-Switching Control Circuitry. A 2.2µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 6, 7, 10, 31, 40).

FB5 (Pin 35): Boost Regulator Feedback Pin. Receives feedback by a resistor divider connected across the output.

FB6 (Pin 36): Buck-Boost Regulator Feedback Pin. Receives feedback by a resistor divider connected across the output.

ENBB (Pin 37): Buck-Boost Regulator Enable Input. Active high. This pin is a high impedance input; do not float.

SWAB6 (Pin 38): Buck-Boost Regulator Switch Pin. External inductor connects to this pin and SWCD6.

SCL (Pin 39): Clock Line for I^2C Port.

V_{IN} (Pin 40): Buck-Boost Regulator Input Supply. A 10µF decoupling capacitor to GND is recommended. Must be connected to all other V_{IN} supply pins (Pins 6, 7, 10, 31, 34).

DV_{CC} (Pin 41): Supply Pin for I^2C Port.

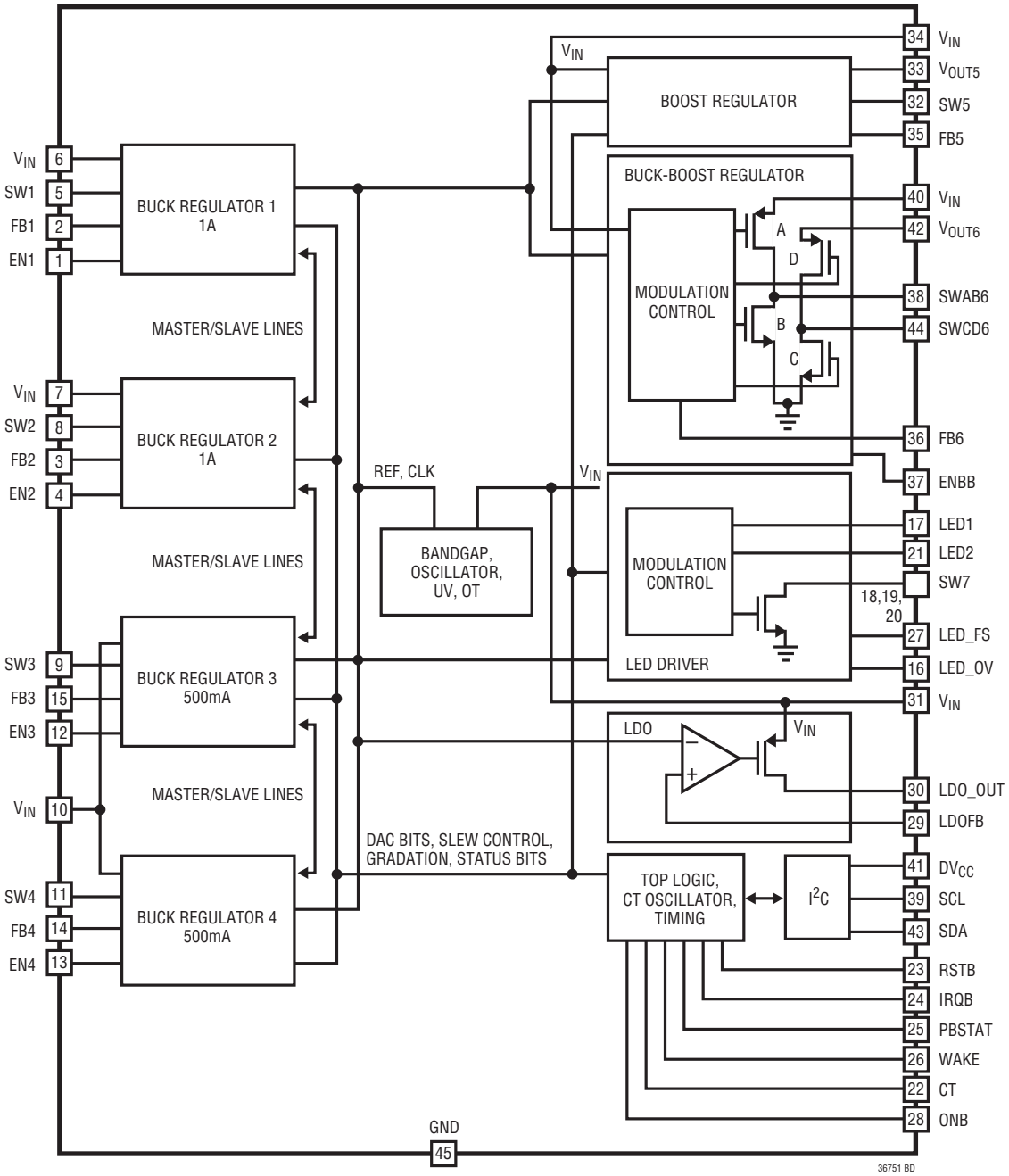
V_{OUT6} (Pins 42): Buck-Boost Regulator Output. Connect a 22µF capacitor to GND.

SDA (Pin 43): Serial Data Line for I^2C Port. Open drain output during readback.

SWCD6 (Pin 44): Buck-Boost Regulator Switch Pin. External inductor connects to this pin and SWAB6.

GND (Exposed Pad Pin 45): Ground for Entire Chip. Must be soldered to PCB for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3675/LTC3675-1 have six monolithic synchronous switching regulators and a dual string boost LED driver and is designed to operate from a single Li-Ion battery. All of the switching regulators and the LED driver are internally compensated and need only external feedback resistors for regulation. The switching regulators also offer two operating modes: Burst Mode operation for higher efficiency at light loads and pulse-skipping/PWM mode. In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into sleep, during which the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping conserve battery power. When the output capacitor droops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases.

All switching regulators and LED driver may be configured via I^2C, providing the user with the flexibility to operate the LTC3675/LTC3675-1 in the most efficient manner. I^2C commands can also be read back via the I^2C port, to ensure a command was not corrupted during a transmission.

All the regulators can be enabled via I^2C commands. The buck regulators and the buck-boost regulator may also be enabled via enable pins. The enable pins have two different enable threshold voltages that depend on the operating state of the LTC3675/LTC3675-1. With all regulators disabled, the enable pin threshold is at 650mV. If any regulator is enabled either by its enable pin or an I^2C command, then the enable pin thresholds are at 400mV. A precision comparator detects a voltage greater than 400mV on the enable pin and turns that regulator on. This precision threshold may be used to sequentially enable regulators. If all regulators are disabled, all the command registers are set in their default state.

There are also 2 bytes of data that report any fault conditions on the LTC3675/LTC3675-1 via I^2C read back.

BUCK SWITCHING REGULATOR

The LTC3675/LTC3675-1 contain four buck regulators. Two of the buck regulators are designed to deliver up to 1A load current each while the other two regulators can deliver up to 500mA each.

The buck regulators can operate in either of two modes. In pulse-skipping mode, the regulator will skip pulses at light loads but will operate at a constant frequency of 2.25MHz at higher loads. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate at constant frequency PWM mode of operation, much the same as pulse-skipping mode at high load. In shutdown, an I^2C control bit provides the flexibility to either keep the SW node in a high impedance state or pull the SW node to GND through a 10k resistor.

The buck regulators have forward and reverse current limiting, soft-start to limit inrush current during start-up, short-circuit protection and slew rate control for lower radiated EMI.

Each buck regulator may be enabled via its enable pin or I^2C. The mode of operation, the feedback regulation voltage and switch slew rate can all be controlled via I^2C. For applications that require higher power, buck regulators may be combined together.

BUCK REGULATORS WITH COMBINED POWER STAGES

Two adjacent buck regulators may be combined in a master-slave configuration by connecting their SW pins together and connecting the higher numbered buck's FB pin to the input supply. The lower numbered buck is always the master. The higher numbered buck is a slave and its enable pin must be tied to ground. In Figure 1, buck

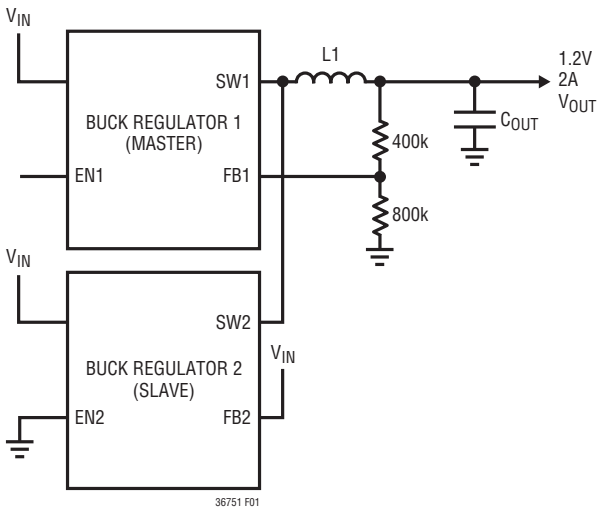


Figure 1. Buck Regulators Configured as Master-Slave

OPERATION

regulator 1 is the master. The feedback network connected to the FB1 pin programs the output voltage to 1.2V. The FB2 pin is tied to V_{IN}, which configures buck regulator 2 as the slave. The SW1 and SW2 pins must be tied together. The register contents of the master program the combined buck regulator's behavior and the register contents of the slave are ignored. The slave buck control circuitry draws no current. The enable of the master buck (EN1) controls the operation of the combined bucks.

Buck regulators 2 and 3 may be configured as combined buck regulators capable of delivering up to 1.5A load current with buck regulator 2 being the master. Buck regulators 3 and 4 may be configured as combined buck regulators capable of delivering up to 1A load current with buck regulator 3 being the master.

BOOST SWITCHING REGULATOR

The boost regulator is capable of delivering up to 1A load current for a programmed output voltage of up to 5V. The boost regulator may be enabled only via I^2C. The mode of operation, feedback regulation voltage and switch slew rate can all be controlled via I^2C.

The boost regulator can operate in either PWM mode or in Burst Mode operation. In PWM operating mode, the regulator operates at a constant frequency of 2.25MHz and provides a low noise solution. For light loads, Burst Mode operation offers improved efficiency. The boost regulator has forward and reverse current limiting, soft-start to limit inrush current during start-up, short-circuit protection and slew rate control for lower radiated EMI. The boost regulator also features true output disconnect when in shutdown. In shutdown, an internal 10k resistor pulls the output to GND.

BUCK-BOOST SWITCHING REGULATOR

The buck-boost regulator is a 2.25MHz voltage mode regulator. The buck-boost regulator is capable of delivering up to 1A load current for a programmed output voltage of 3.3V. The regulator can be enabled via its enable pin or via I^2C. The mode of operation, feedback regulation voltage and switch slew rate can all be controlled via I^2C.

The buck-boost regulator can operate in either PWM mode or in Burst Mode operation. The PWM operating mode provides a low noise solution. For light loads, Burst Mode operation offers improved efficiency. The buck-boost regulator has forward current limiting, soft-start to limit inrush current during start-up, short-circuit protection and slew rate control for lower radiated EMI.

When the output voltage is below 2.65V (typical) during start-up, Burst Mode operation is disabled and switch D is turned off. The forward current is carried by the switch D well diode and there is no reverse current flowing in this condition. In shutdown, an internal 10k resistor pulls the output to GND.

LED DRIVER

The LED driver uses a constant frequency, current mode boost converter to supply power to up to two strings of 10 series LEDs. The series string of LEDs is connected from the output of the boost converter to an LED pin. The LED pin is a programmable constant current sink. The boost converter will regulate its output to force the LED pin to 300mV. The percentage of full-scale current sunk by the LED pin is programmed via I^2C.

The LED boost converter is designed for very high duty cycle operation and can boost from below 3V to 40V out at up to 55mA. The LED boost also features an overvoltage protection feature to limit the output voltage in case of an open circuit in an LED string. The boost converter will operate in either continuous conduction mode, discontinuous conduction mode or pulse-skipping mode depending on the inductor current required for regulation. The boost converter may also be configured to operate as an independent high voltage boost regulator via I^2C. The LED driver may also be configured as a single string LED driver. When driving a single string, LED1 and LED2 should be tied together.

The LED driver features a fully automatic gradation circuit. This circuit allows the current to ramp up or down at a controlled rate between any two current levels. On power-up the LED DAC register is set to 0. To enable the LED driver a non-zero value must be programmed into this register.

OPERATION

The gradation circuit will then ramp the current to the programmed value at a rate determined by the gradation rate bits. Once the LED driver reaches this value it will regulate that current until programmed otherwise. If a new value is programmed in the LED brightness register, the LED driver's current will ramp up or down at the programmed rate until that current is reached. To disable the LED driver, a code of zero is programmed in the LED DAC register. The gradation circuit will then ramp the current down at the programmed rate. Once the current reaches zero the gradation circuit will disable the boost and the entire LED driver will enter shutdown mode.

The LED driver is protected by the LED_OV pin. This pin acts as a secondary feedback path that limits the voltage on the output capacitor. A feedback divider is placed from the LED boost's output to the LED_OV pin. Values for this divider are selected to limit the output voltage similarly to the feedback dividers discussed in "Switching Regulator Output Voltage and Feedback Network" in the Applications Information section. The LED driver begins to transition to LED_OV control at 800mV and is fully controlled by the LED_OV pin by 825mV. During this transition the LED pins will begin to drop out of regulation. For this reason during normal operation the voltage on this pin should be kept below 800mV.

The LED driver is also designed to limit the maximum voltage on the LED1 and LED2 pins to no more than 8V. The boost regulates the minimum voltage on either LED pin. If one of the LED pins is shorted to ground the boost will only drive the other LED pin up to the voltage clamp, or the LED_OV voltage, whichever is lower. If one LED string is shorted, or partially shorted, this clamp will prevent the boost from damaging the LED pin.

PUSHBUTTON INTERFACE AND POWER-UP POWER-DOWN SEQUENCING

The LTC3675/LTC3675-1 provide pushbutton functionality to either power up or power down the part. The ONB, WAKE and PBSTAT pins provide the user with flexibility to power up or power down the part in addition to having I^2C control. All PB timing parameters are scaled using the CT pin. Times described below apply to a nominal C_T of 0.01µF.

The LTC3675/LTC3675-1 are in an off state when it is powered up with all regulators in shutdown. The WAKE pin is LOW in the off state. The WAKE pin will go HIGH either if ONB is pulled LOW for 400ms or a regulator is enabled via its enable pin or an I^2C command. The WAKE pin stays in its HIGH state for 5 seconds and then gets pulled low. WAKE will not go HIGH again if a second regulator is subsequently enabled. The LTC3675/LTC3675-1 are in an on state if either the WAKE pin is HIGH or a regulator is enabled.

The PBSTAT pin reflects the status of the ONB when the LTC3675/LTC3675-1 are in an on state. Once in the on state, the LTC3675/LTC3675-1 can be powered down by holding ONB LOW for at least 5 seconds. All enabled regulators will be turned off for 1 second and the contents of the program registers are reset to their default state. This manner of power-down is called a hard reset. A hard reset may also be generated by using an I^2C command.

POWER-UP AND POWER-DOWN VIA PUSHBUTTON

The LTC3675/LTC3675-1 may be turned on and off using the WAKE pin as shown in Figures 2a and 2b. In Figures 2a and 2b, pressing ONB low at time t_1, causes the WAKE pin to go high at time t_2 and stay high for 5 seconds, after which WAKE is pulled low. WAKE going HIGH at t_2 causes buck regulator 1 to power up, which sequentially powers up the other buck regulators. The RSTB pin gets pulled HIGH 200ms after the last enabled buck is in its PGOOD state. An application showing sequential regulator start-up is shown in the Typical Applications section (Figure 7).

If an I^2C command is written before the 5 second WAKE period t_3 to keep the buck regulators enabled, the regulators stay enabled as shown in Figure 2b. Otherwise, when WAKE gets pulled low at t_3, the buck regulators will also power down sequentially as shown in Figure 2a.

In Figure 2b, ONB is held LOW at instant t_4 for 5 seconds. This causes a hard reset to be generated and at t_5, all regulators are powered down.

OPERATION

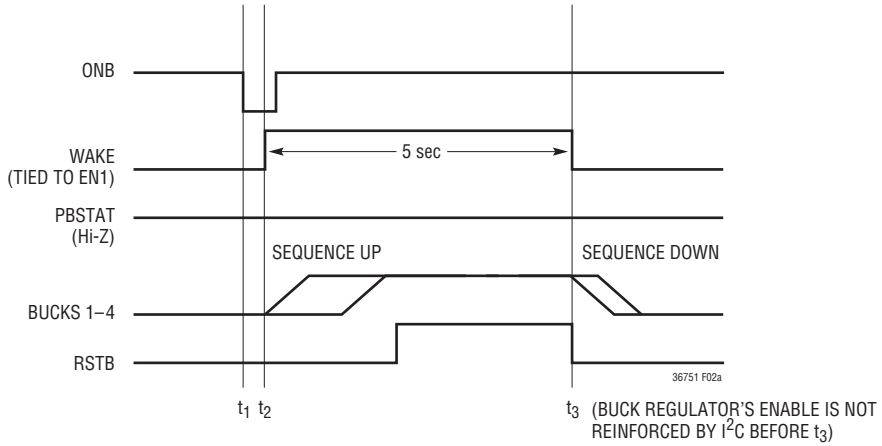


Figure 2a. Power-Up Using WAKE (Sequenced Power-Up, Figure 7)

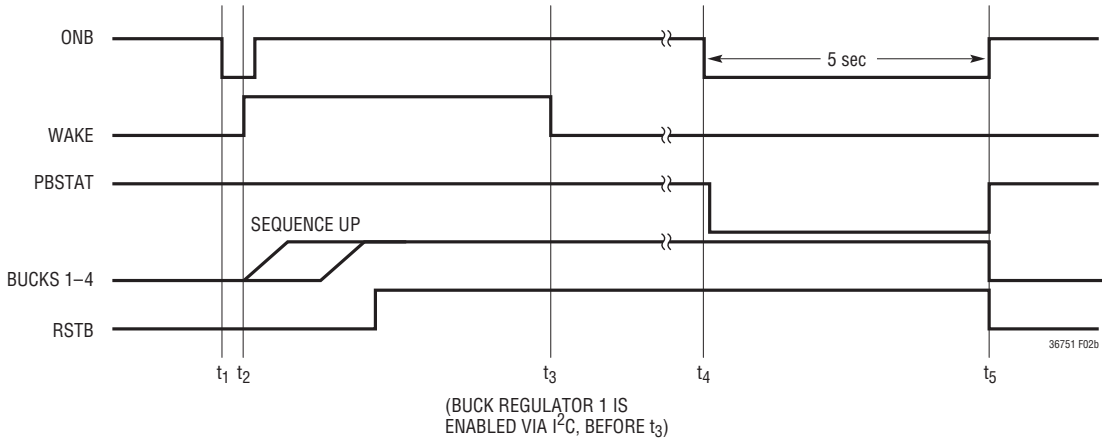


Figure 2b. Power-Up Using WAKE and Power-Down Due to Hard Reset (Sequenced Power-Up, Figure 7)

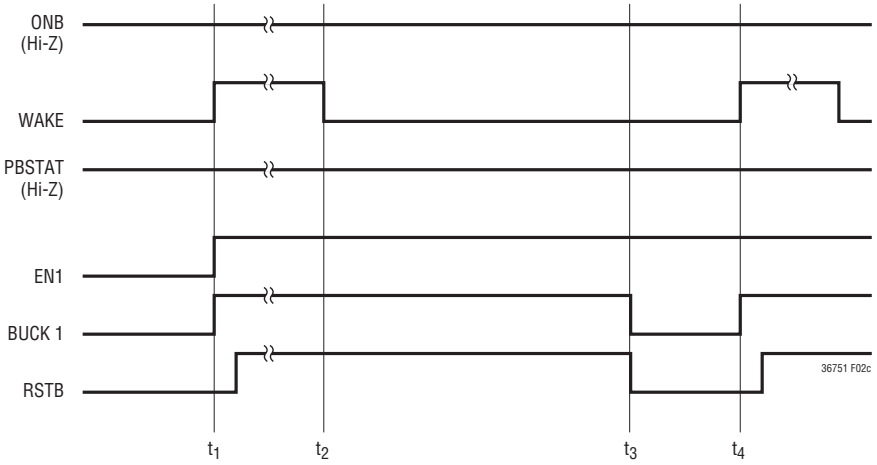


Figure 2c. Power-Up Using an Enable Pin and Power-Down Due to I2C Generated Hard Reset

OPERATION

POWER-UP AND POWER-DOWN VIA ENABLE PIN OR I²C

With the LTC3675/LTC3675-1 in its off state, a regulator can be enabled either via its enable pin or I²C. In Figure 2c, buck regulator 1 is enabled via its enable pin at time t_1. The WAKE pin goes HIGH for 5 seconds and at t_2 is pulled LOW. The buck regulator stays enabled until time t_3 when a hard reset command is issued via I²C. The buck regulator powers down and stays off for 1 second. At time t_4, the LTC3675/LTC3675-1 exit from the power down state. Since the buck regulator 1 is still enabled via its enable pin, it powers back up. WAKE also gets pulled HIGH for 5 seconds. The RSTB pin gets pulled HIGH 200ms after the buck regulator 1 is in its PGOOD state.

LED CURRENT PROGRAMMING

The LED current is primarily controlled through the LED DAC register at I²C sub-address 8. This register controls an 8 bit current DAC. A 20k resistor placed between the LED_FS pin and ground provides a current reference for the DAC which results in 98µA of programmed LED current per LSB. For example, programming a LED DAC register code of 64h will result in a LED current of 9.8mA and a full-scale setting of FFh will result in a LED current of 25mA.

The 2xFS bit which is bit 3 of the LED configuration register at sub-address 7 effectively doubles the programmed LED current. With a 20k resistor from LED_FS to ground each LSB will be 196µA. Programming a LED DAC register code of 64h will result in a LED current of 19.6mA and a full-scale setting of FFh will result in an LED current of 50mA. The 2xFS mode is only intended for use when the output voltage is below 20V.

I²C INTERFACE

The LTC3675/LTC3675-1 may communicate with a bus master using the standard I²C 2-wire interface. The timing diagram (Figure 3) shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC3675/LTC3675-1 are both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below 1V, the I²C serial port is cleared and the LTC3675/LTC3675-1 registers are set to their default configurations.

I²C Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

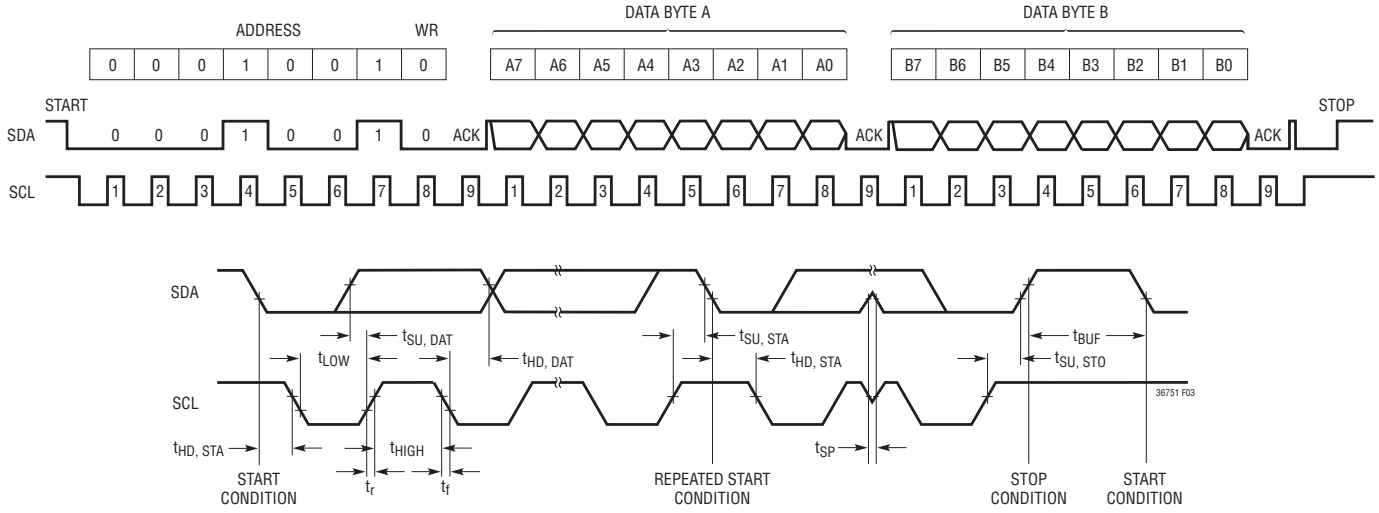


Figure 3. I²C Bus Operation

OPERATION

I²C Start and Stop Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3675/LTC3675-1, the master may transmit a STOP condition which commands the LTC3675/LTC3675-1 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3675/LTC3675-1 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3675/LTC3675-1 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3675/LTC3675-1 are written to (write address), it acknowledges its write address as well as the subsequent two data bytes. When it is read from (read address), the LTC3675/LTC3675-1 acknowledge its read address only. The bus master should acknowledge receipt of information from the LTC3675/LTC3675-1.

An acknowledge (active LOW) generated by the LTC3675/LTC3675-1 lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC3675/LTC3675-1 pull down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC3675/LTC3675-1 are read from, it releases the SDA line so that the master may acknowledge receipt of the data. Since the LTC3675/LTC3675-1 only transmit one byte of data during a read cycle, a master not acknowledging the data sent by the LTC3675/LTC3675-1 has no I²C specific consequence on the operation of the I²C port.

I²C Slave Address

The LTC3675 responds to a 7-bit address which has been factory programmed to b'0001001[R/WB]'. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC3675 and 1 when reading data from it. Considering the address as an 8-bit word, the write address is 12h and the read address is 13h. The LTC3675-1 is factory programmed to b'0110100[R/WB]'. Its write address is 68h and the read address is 69h.

The LTC3675/LTC3675-1 will acknowledge both the read and write addresses.

I²C Sub-Addressed Writing

The LTC3675/LTC3675-1 have twelve command registers for control input. They are accessed by the I²C port via a sub-addressed writing system.

A single write cycle of the LTC3675/LTC3675-1 consists of exactly three bytes except when a clear interrupt command is written. The first byte is always the LTC3675/LTC3675-1's write address. The second byte represents the sub-address. The sub-address is a pointer which directs the subsequent data byte within the LTC3675/LTC3675-1. The third byte consists of the data to be written to the location pointed to by the sub-address. The LTC3675/LTC3675-1 contain 11 control registers which can be written to.

I²C Bus Write Operation

The master initiates communication with the LTC3675/LTC3675-1 with a START condition and the appropriate write address. If the address matches that of the LTC3675/LTC3675-1, the LTC3675/LTC3675-1 return an acknowledge. The master should then deliver the sub-address. Again the LTC3675/LTC3675-1 acknowledge and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3675/LTC3675-1. This procedure must be repeated for each sub-address that requires new data. After one or more cycles of [ADDRESS][SUB-ADDRESS][DATA], the master may terminate the communication with a STOP condition. Multiple sub addresses may be written to with a single address command using a

OPERATION

Table 1. Summary of I²C Sub-Addresses and Byte Formats. Bits A7, A6, A5, A4 of Sub-Address Need to Be 0 to Access Registers

SUB-ADDRESS A7A6A5A4A3A2A1A0	OPER-ATION	ACTION	BYTE FORMAT D7D6D5D4D3D2D1D0	DEFAULT D7D6D5D4D3D2D1D0	COMMENTS
0000 0000 (00h)	Write	No Register Selected			Used in the Clear Interrupt Operation.
0000 0001 (01h)	Read/ Write	Buck1 Register	Enable, OUT_Hi-Z, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	01101111	
0000 0010 (02h)	Read/ Write	Buck2 Register	Enable, OUT_Hi-Z, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	01101111	
0000 0011 (03h)	Read/ Write	Buck3 Register	Enable, OUT_Hi-Z, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	01101111	
0000 0100 (04h)	Read/ Write	Buck4 Register	Enable, OUT_Hi-Z, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	01101111	
0000 0101 (05h)	Read/ Write	Boost Register	Enable, Unused, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	00001111	
0000 0110 (06h)	Read/ Write	Buck-Boost Register	Enable, Unused, Mode, Slow, DAC[3], DAC[2], DAC[1], DAC[0]	00001111	
0000 0111 (07h)	Read/ Write	LED Configuration Register	Unused, Mode[1], Mode[0], Slow, 2XFS, GRAD[2], GRAD[1], GRAD[0]	00001111	
0000 1000 (08h)	Read/ Write	LED DAC Register	DAC[7], DAC[6], DAC[5], DAC[4], DAC[3], DAC[2], DAC[1], DAC[0]	00000000	00000000 = LED Driver Disabled 11111111 = 25mA per String
0000 1001 (09h)	Read/ Write	UVOT Register	RESET_ALL, UV[2], UV[1], UV[0], UNUSED, UNUSED, OT[1], OT[0]	00000000	
0000 1010 (0Ah)	Read/ Write	RSTB Mask Register	UNUSED, PGOOD[7], PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]	11111111	Fault will pull RSTB low if the corresponding bit is '1'
0000 1011 (0Bh)	Read/ Write	IRQB Mask Register	UNUSED, PGOOD[7], PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]	00000000	Fault will pull IRQB low if the corresponding bit is '1'
0000 1100 (0Ch)	Read	Status Register (Real Time)	UNUSED, UNUSED, PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]		Read Back
0000 1101 (0Dh)	Read	Status Register (Latched)	UV, OT, PGOOD[6], PGOOD[5], PGOOD[4], PGOOD[3], PGOOD[2], PGOOD[1]		Read Back
0000 1111 (0Fh)	Write	Clear Interrupt			Clears the Interrupt Bit, Status Latches are Unlatched

[ADDRESS][SUB-ADDRESS][DATA][SUB-ADDRESS][DATA] sequence. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3675/LTC3675-1 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3675/LTC3675-1 will update its command latches with the data that it had received.

It is important to understand that until a STOP signal is transmitted, data written to the LTC3675/LTC3675-1 command registers are not acted on by the LTC3675/LTC3675-1. Only once a STOP signal is issued is the data transferred to the command latch and acted on. The one exception is when sub-address 0Fh is written to clear an interrupt. To clear an interrupt, sub address 0Fh must be written, followed by sub address 00h. A complete clear interrupt cycle would have the following write sequence: 12h, 0Fh, STOP, 12h, 00h, STOP.

I²C Bus Read Operation

The LTC3675/LTC3675-1 have eleven command registers and two status registers. The contents of any of these registers may be read back via I²C.

To read the data of a register, that register's sub-address must be provided to the LTC3675/LTC3675-1. The bus master reads the status of the LTC3675/LTC3675-1 with a START condition followed by the LTC3675/LTC3675-1's write address followed by the first data byte (the sub-address of the register whose data needs to be read) which

OPERATION

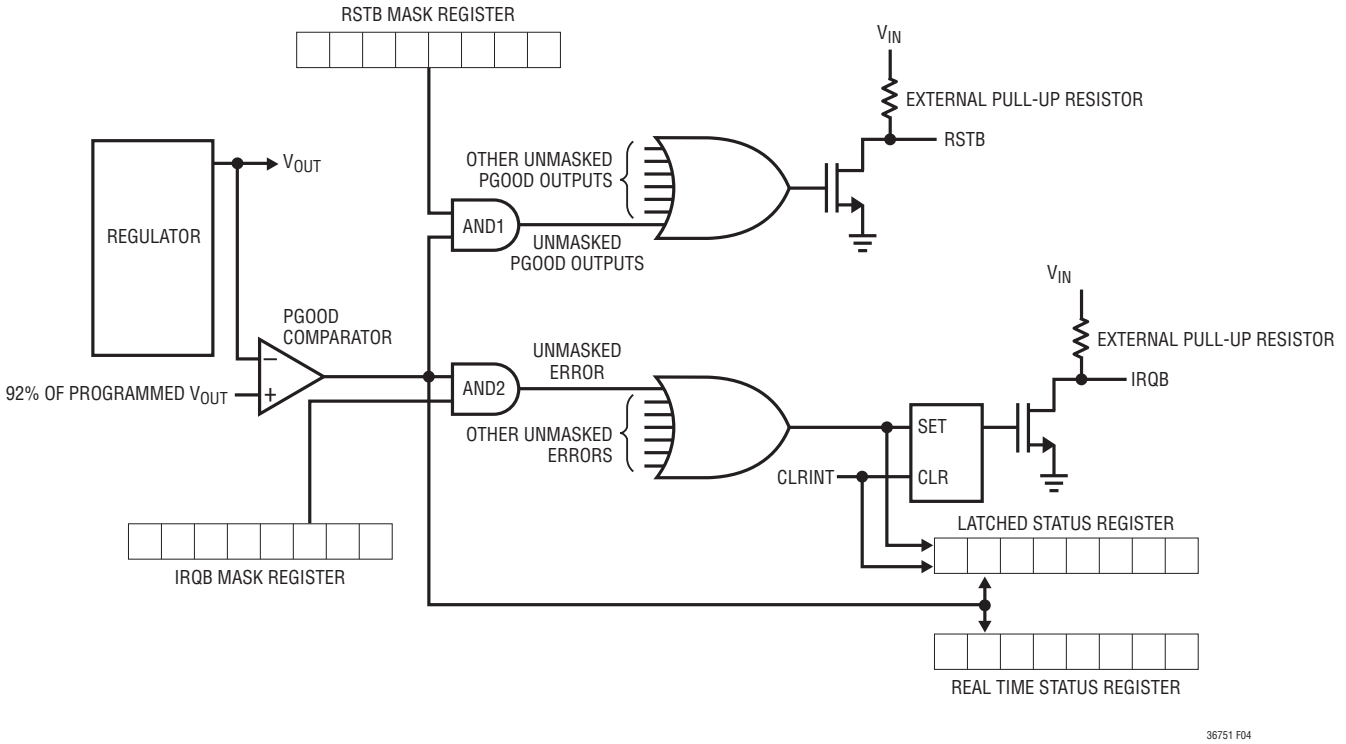


Figure 4. Simplified Schematic Showing RSTB and IRQB Signal Path

is acknowledged by the LTC3675/LTC3675-1. After receiving the acknowledge signal from the LTC3675/LTC3675-1 the bus master initiates a new START condition followed by the LTC3675/LTC3675-1 read address. The LTC3675/LTC3675-1 acknowledge the read address and then return a byte of read back data from the selected register. A STOP command is not required for the bus read operation.

Immediately after writing data to a register, the contents of that register may be read back if the bus master issues a START condition followed by the LTC3675/LTC3675-1 read address.

ERROR CONDITION REPORTING VIA RSTB AND IRQB PINS

Error conditions are reported back via the IRQB and RSTB pins. After an error condition is detected, status data can be read back to a microprocessor via I^2C to determine the exact nature of the error condition.

Figure 4 is a simplified schematic showing the signal path for reporting errors via the RSTB and IRQB pins.

All the switching regulators and the LED driver have an internal power good (PGOOD) signal. When the regulated output voltage of an enabled switcher rises above 93.5% of its programmed value, the PGOOD signal will transition high. When the regulated output voltage falls below 92.5% of its programmed value, the PGOOD signal is pulled low. If that PGOOD is not masked and stays low for greater than 50µs, then it pulls the RSTB and IRQB pins low, indicating to a microprocessor that an error condition has occurred. The 50µs filter time prevents the pins from being pulled low due to a transient.

The LED driver has a PGOOD signal (PGOOD[7]) that is used to indicate output voltage status only when it is configured as a high voltage boost regulator. In all other operating modes, PGOOD[7] is disabled.

An error condition that pulls the RSTB pin low is not latched. When the error condition goes away, the RSTB pin is released and is pulled high if no other error condition exists.

In addition to the PGOOD signals of the regulators, the IRQB pin also indicates the status of the overtemperature

OPERATION

and undervoltage flags. The undervoltage and overtemperature faults cannot be masked. A fault that causes the IRQB pin to be pulled low is latched. When the fault condition is cleared, the IRQB pin is still maintained in its low state. The user needs to clear the interrupt by using a CLRINT command.

On start-up, all PGOOD outputs are unmasked and a power-on reset will cause RSTB to be pulled low. Once all enabled regulators have their output PGOOD for 200ms typical (C_T = 0.01µF) the RSTB output goes Hi-Z.

By masking a PGOOD signal, the RSTB or IRQB pin will remain Hi-Z even though the output voltage of a regulator may be below its PGOOD threshold. However, when the status register is read back, the true condition of PGOOD is reported.

UNDERVOLTAGE AND OVERTEMPERATURE FUNCTIONALITY

The undervoltage (UV) circuit monitors the input supply voltage and shuts down all enabled regulators if the input voltage falls below 2.45V. The LTC3675/LTC3675-1 also provide a user with an undervoltage warning, which indicates to the user that the input supply voltage is approaching the UV threshold. The undervoltage warning threshold is user programmable as shown in Table 2.

Table 2. UV Warning Thresholds

UV[2], UV[1], UV[0]	FALLING V_{IN} WARNING THRESHOLD
000 (Default)	2.7V
001	2.8V
010	2.9V
011	3.0V
100	3.1V
101	3.2V
110	3.3V
111	3.4V

To prevent thermal damage to the LTC3675/LTC3675-1 and its surrounding components, the LTC3675/LTC3675-1 incorporate an overtemperature (OT) function. When the die temperature reaches 150°C all enabled regulators are shut down and remain in shutdown until the die temperature falls to 135°C. The LTC3675/LTC3675-1 also have an overtemperature warning function which warns a user that the die temperature is approaching the OT threshold which allows the user to take any corrective action. The OT warning threshold is user programmable as shown in Table 3.

Table 3. OT Warning Thresholds

OT[1], OT[0]	OT WARNING THRESHOLD
00 (Default)	10° Below OT
01	20° Below OT
10	30° Below OT
11	40° Below OT

A UV or OT warning is reported to the user when the IRQB pin is in its high impedance state. The UV and OT warning flags are not maskable by the user.

RESET_ALL Functionality: The RESET_ALL bit shuts down all enabled regulators (enabled either via its enable pin or I^2C) for 1 second. All command registers are cleared and put in their default state.

APPLICATIONS INFORMATION

Switching Regulator Output Voltage and Feedback Network

The output voltage of the switching regulators is programmed by a resistor divider connected from the switching regulator's output to its feedback pin and is given by $V_{OUT} = V_{FB} (1 + R2/R1)$ as shown in Figure 5. Typical values for R1 range from 40kΩ to 1MΩ. The buck regulator transient response may improve with optional capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response.

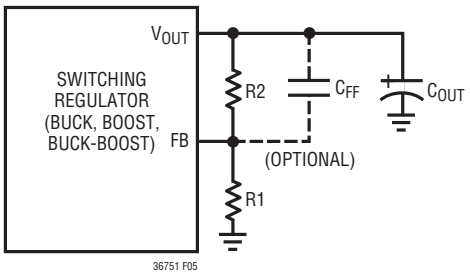


Figure 5. Feedback Components

Buck Regulators

All four buck regulators are designed to be used with 2.2µH inductors. Tables 4 and 5 show the recommended inductors for the 500mA and 1A buck regulators.

The input supply needs to be decoupled with a 10µF capacitor while the output needs to be decoupled with a 22µF capacitor for a 1A buck regulator and 10µF for a 500mA buck regulator. Refer to Capacitor Selection in the Applications Information section for details on selecting a proper capacitor.

Each buck regulator can be programmed via I^2C. To program buck regulator 1 (1A) use sub-address 01h, buck regulator 2 (1A) sub-address 02h, buck regulator 3 (500mA) sub-address 03h and buck regulator4 (500mA) sub-address 04h. The bit format is explained in Table 6.

Combined Buck Regulators

A single 2A buck regulator is available by combining both 1A buck regulators together. Both the 500mA buck regulators may also be combined together to form a 1A buck regulator. Tables 4 and 7 show the recommended inductors.

The input supply needs to be decoupled with a 22µF capacitor while the output needs to be decoupled with

Table 4. Recommended Inductors for 1A Buck Regulators and Ganged Buck 3, Buck 4 Application

PART NUMBER	L(µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018-222	2.2	2.8	70	4 × 4 × 1.8	Coilcraft www.coilcraft.com
XFL4022-222	2.2	3.5	21.35	4 × 4 × 2	Coilcraft www.coilcraft.com
LTF5022-2R2	2.2	3.2	36	5 × 5.2 × 2.2	TDK www.tdk.com
LPS3015-222	2.2	2.0	110	3 × 3 × 1.5	Coilcraft www.coilcraft.com

Table 5. Recommended Inductors for 500mA Buck Regulators

PART NUMBER	L(µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS3015-222	2.2	2.0	110	3 × 3 × 1.5	Coilcraft www.coilcraft.com
MLPS3015-2R2	2.2	1.4	110	3 × 3 × 1.5	Maglayers www.maglayers.com
MDT2520-CR2R2	2.2	1.35	90	2.5 × 2 × 1	Toko www.toko.com
LQM2HPN2R2	2.2	1.0	120	2.5 × 2 × 1.1	Murata www.murata.com

APPLICATIONS INFORMATION

a 47µF capacitor for a 2A combined buck regulator and 22µF for a 1A combined buck regulator. Refer to "Capacitor Selection" in the Applications Information section for details on selecting a proper capacitor.

Boost Regulator

The boost regulator is designed to be used with a 2.2µH inductor. Table 8 provides a list of recommended inductors.

The input supply needs to be decoupled with a 10µF capacitor while the output needs to be decoupled with two 22µF capacitors. Refer to Capacitor Selection in the Applications Information section for details on selecting a proper capacitor.

The boost regulator can be programmed via I^{2}C. To program the boost regulator, use sub-address 05h. The bit format is explained in Table 9.

Table 6. Buck Regulator Program Register Bit Format

Bit7	Enable	Default is '0' which disables the part. A buck regulator can also be enabled via its enable pin. When enabled via pin, the contents of the I^{2}C register program its functionality.
Bit6	OUT_Hi-Z	Default is '1' in which the SW node remains in a high impedance state when the regulator is in shutdown. A '0' pulls the SW node to GND through a 10k resistor.
Bit5	Mode	Default is '1' which is Burst Mode operation. A '0' programs the regulator to operate in pulse-skipping mode.
Bit4	Slow Edge	This bit controls the slew rate of the switch node. Default is '0' which enables the switch node to slew at a faster rate, than if the bit were programmed a '1'.
Bit3(DAC3) Bit2(DAC2) Bit1(DAC1) Bit0(DAC0)	DAC Control	These bits are used to program the feedback regulation voltage. Default is '1111' which programs a full-scale voltage of 800mV. Bits '0000' program the lowest feedback regulation of 425mV. A LSB (DAC0) has a bit weight of 25mV.

Table 7. Recommended Inductors for 2A Combined Buck Regulator

PART NUMBER	L(µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XFL4022-222	2.2	3.5	21.35	4 × 4 × 2	Coilcraft www.coilcraft.com
LPS6225-222	2.2	4	45	6 × 6 × 2.5	Coilcraft www.coilcraft.com
FDV0530-2R2	2.2	5.3	17.3	6.2 × 5.8 × 3	Toko www.toko.com

Table 8. Recommended Inductors for Boost Regulator and Buck-Boost Regulator

PART NUMBER	L(µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XFL4022-222	2.2	3.5	21.35	4 × 4 × 2	Coilcraft www.coilcraft.com
LTF5022-2R2	2.2	3.2	36	5 × 5.2 × 2.2	TDK www.tdk.com

Table 9. Boost Regulator Program Register Bit Format

Bit7	Enable	Default is '0' which disables the boost.
Bit6	x	Unused
Bit5	Mode	Mode = 0 is PWM mode, Mode = 1 is Burst Mode operation
Bit4	Slow Edge	This bit controls the slew rate of the switch node. Default is '0' which enables the switch node to slew at a faster rate than if the bit were programmed a '1.'
Bit3(DAC3) Bit2(DAC2) Bit1(DAC1) Bit0(DAC0)	DAC Control	These bits are used to program the feedback regulation voltage. Default is '1111' which programs a full-scale voltage of 800mV. Bits '0000' program the lowest feedback regulation of 425mV. A LSB (DAC0) has a bit weight of 25mV.

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Optional capacitor C_{FF} is not needed and may compromise loop stability.

Buck-Boost Regulator

The buck-boost regulator is an internally compensated voltage mode regulator that is designed to be used with a 2.2µH inductor. Recommended inductors are listed in the Table 8.

The input supply needs to be decoupled with a 10µF capacitor while the output needs to be decoupled with a 22µF capacitor. Refer to "Capacitor Selection" in the Applications Information section for details on selecting a proper capacitor.

The buck-boost regulator can be programmed via I^2C. To program the buck-boost regulator, use sub-address 06h. The bit format is explained in Table 10.

To ensure loop stability, feedback resistor R1 in Figure 5 should be no greater than 105kΩ. Optional capacitor C_{FF} is not needed and may compromise loop stability.

LED Driver

For proper operation the LED driver boost circuit needs a 10µH inductor. Recommended inductors are listed in Table 11.

The LED driver also needs a rectifier diode. Recommended schottky diodes are listed in Table 12.

The LED driver has two registers that can be programmed via I^2C. One of the registers is accessed at sub-address 07h and the bit format is as shown in Table 13.

The rate at which the gradation circuit ramps the LED current is set by GRAD[2:0]. GRAD[2:0] sets the time the LED driver will take to transition through one LSB of LED current.

Table 10. Buck-Boost Regulator Program Register Bit Format

Bit7	Enable	Default is '0' which disables the buck-boost. The buck-boost regulator can alternately be enabled via its enable pin. When enabled via pin, the contents of the I^2C register program its functionality.
Bit6	x	Unused
Bit5	Mode	Mode = 0 is PWM mode, Mode = 1 is Burst Mode operation. Default is '0.'
Bit4	Slow edge	This bit controls the slew rate of the switch node. Default is '0' which enables the switch node to slew at a faster rate than if the bit were programmed a '1.'
Bit3(DAC3) Bit2(DAC2) Bit1(DAC1) Bit0(DAC0)	DAC control	These bits are used to program the feedback regulation voltage. Default is '1111' which programs a full-scale voltage of 800mV. Bits '0000' program the lowest feedback regulation of 425mV. A LSB (DAC0) has a bit weight of 25mV.

Table 11. Recommended Inductors for LED Driver

PART NUMBER	L(µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS6225-103M	10	2.1	105	6 × 6 × 2.5	Coilcraft www.coilcraft.com
IHLP2020BZER10RM01	10	4	184	5.2 × 5.5 × 2	Vishay www.vishay.com

Table 12. Recommended Schottky Diodes for LED Driver

PART NUMBER	I_F (A)	MANUFACTURER
PD3S140	1.0	Diodes Inc. www.diodes.com
ZLLS1000	1.16	Diodes Inc./Zetex www.diodes.com
CTLSH1-40M322	1.0	Central Semiconductor www.centralsemi.com

APPLICATIONS INFORMATION

Table 13. LED Driver Regulator Program Register 1 Bit Format

Bit7	x	Unused
Bit6 Bit5	Mode1 Mode0	Mode1 = Mode0 = 0 is default; both LED pins are regulated. Mode1 = 0 Mode0 = 1; Only LED1 is regulated. (Single string application). Mode1 = 1 Mode0 = 0; LED driver is configured as a high voltage boost regulator. Mode1 = Mode0 = 1; Both LED pins are regulated, but boost is not powered up. In this mode an external voltage is needed to drive the LED's.
Bit4	Slow Edge	This bit controls the slew rate of the switch node. Default is '0' which enables the switch node to slew at a faster rate than if the bit were programmed a '1.'
Bit3	2xFS	This bit doubles the full-scale programmed LED current. Default is '1.'
Bit2(GRAD2) Bit1(GRAD1) Bit0(GRAD0)	DAC Control	LED current gradation timing bits. Default is '111.' See Table 14.

These times are shown in Table 14. The default state of 000 in GRAD[2:0] results in a very fast ramp time that cannot be visually perceived.

Table 14. LED Gradation Bits

GRAD2, GRAD1, GRAD0	GRADATION STEP TIME
000	0.056 ms
001	0.912 ms
010	1.824 ms
011	3.648 ms
100	7.296 ms
101	14.592 ms
110	29.184 ms
111 (Default)	58.368 ms

The LED DAC register is at sub-address 08h. All 8 bits in this register are used to control LED current. The default state of this register is 00h which disables the LED driver. See Table 1.

Operating the LED Driver As a High Voltage Boost Regulator

The LED driver may be configured as a high voltage boost regulator capable of producing an output voltage up to 40V. The boost mode may be programmed via I^2C. In this mode, the LED_OV pin serves as the feedback pin. The feedback resistors are selected as discussed in the Switching Regulator Output voltage and Feedback Network section. The LED_FS pins must be tied to the input supply in this mode. When configured as a high voltage boost, the LED DAC register is ignored.

To maintain stability, the average inductor current must be maintained below 750mA. This limits the deliverable output current at low input supply voltages. Figure 8 gives an example of the LED driver configured as a high voltage boost regulator.

Input and Output Decoupling Capacitor Selection

The LTC3675/LTC3675-1 have multiple input supply pins and output pins. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

The input supply voltage pins 6, 7, 10 and 40 all need to be decoupled with at least 10µF capacitors. The input supply pins 31 and 34 and the DVCC pin 41 need to be decoupled with 2.2µF capacitors. The outputs of the 1A buck regulators need 22µF capacitors, while the outputs of the 500mA buck regulators need 10µF capacitors. The buck-boost output regulator needs a 22µF decoupling capacitor. The boost regulator needs two 22µF output decoupling capacitors. The LED driver output pin should be decoupled with a 4.7µF capacitor.

APPLICATIONS INFORMATION

Choosing the C_T Capacitor

The C_T capacitor may be used to program the timing parameters associated with the pushbutton. For a given C_T capacitor the timing parameters may be calculated as below. C_T is in units of µF.

$t_{ONB\_LO} = 5000 \times C_T$ ms

$t_{PBSTAT\_PW} = 5000 \times C_T$ ms

$t_{ONB\_WAKE} = 40000 \times C_T$ ms

$t_{WAKE\_ON} = 500 \times C_T$ seconds

$t_{ONB\_HR} = 500 \times C_T$ seconds

$t_{HR} = 100 \times C_T$ seconds

Programming the UVOT Register

The UV/OT warning byte (default 0000 0000) structure is as below:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RESET_ALL	UV[2]	UV[1]	UV[0]	Unused	Unused	OT[1]	OT[0]

Programming the RSTB and IRQB Mask Registers

The RSTB mask register can be programmed by the user at sub-address 0Ah and its format is as below.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Unused	PGOOD7	PGOOD6	PGOOD5	PGOOD4	PGOOD3	PGOOD2	PGOOD1

If a bit is set to '1,' then the corresponding regulator's PGOOD will pull RSTB low if a PGOOD fault were to occur. The default for this register is FFh.

The IRQB mask register has the same bit format as the RSTB mask register. The IRQB mask register is located at sub-address 0Bh and its default contents are 00h.

PGOOD7 is used only when the LED driver is configured as a high voltage boost regulator.

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Status Byte Read Back

When either the RSTB or IRQB pin is pulled low, it indicates to the user that a fault condition has occurred. To find out the exact nature of the fault, the user can read the status registers. There are two status registers. One register provides real time fault condition reporting while a second register latches data when an interrupt has occurred. Figure 4 shows the operation of the real time and latched status registers. The contents of the latched status register are cleared when a CLRINT signal is issued. A PGOOD bit is a '0' if that regulator's output voltage is more than 8% below its programmed value.

The sub-address for the real time status register is 0Ch and its format is as follows:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Unused	Unused	PGOOD6	PGOOD5	PGOOD4	PGOOD3	PGOOD2	PGOOD1

The sub-address for the latched status register is 0Dh and its format is as follows:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
UV	OT	PGOOD6	PGOOD5	PGOOD4	PGOOD3	PGOOD2	PGOOD1

A write operation cannot be performed to either of the status registers.

PCB Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3675/LTC3675-1:

1. The exposed pad of the package (pin 45) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. All the input supply pins must be tied together and each supply pin should have a decoupling capacitor.
3. The switching regulator input supply pins and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should

APPLICATIONS INFORMATION

connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It's important to minimize inductance from these capacitors to the V_{IN} pins of the LTC3675/LTC3675-1.

4. The switching power traces connecting SW1, SW2, SW3, SW4, SW5, SWAB6, SWCD6 and SW7 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, high input impedance sensitive nodes such as the feedback nodes and LED_OV node should be kept far away or shielded from the switching nodes or poor performance could result.
5. The GND side of the switching regulator output capacitors should connect directly to the thermal ground plane of the part. Minimize the trace length from the output capacitor to the inductor(s)/pin(s).
6. In a combined buck regulator application the trace length of switch nodes to the inductor must be kept equal to ensure proper operation.

TYPICAL APPLICATIONS

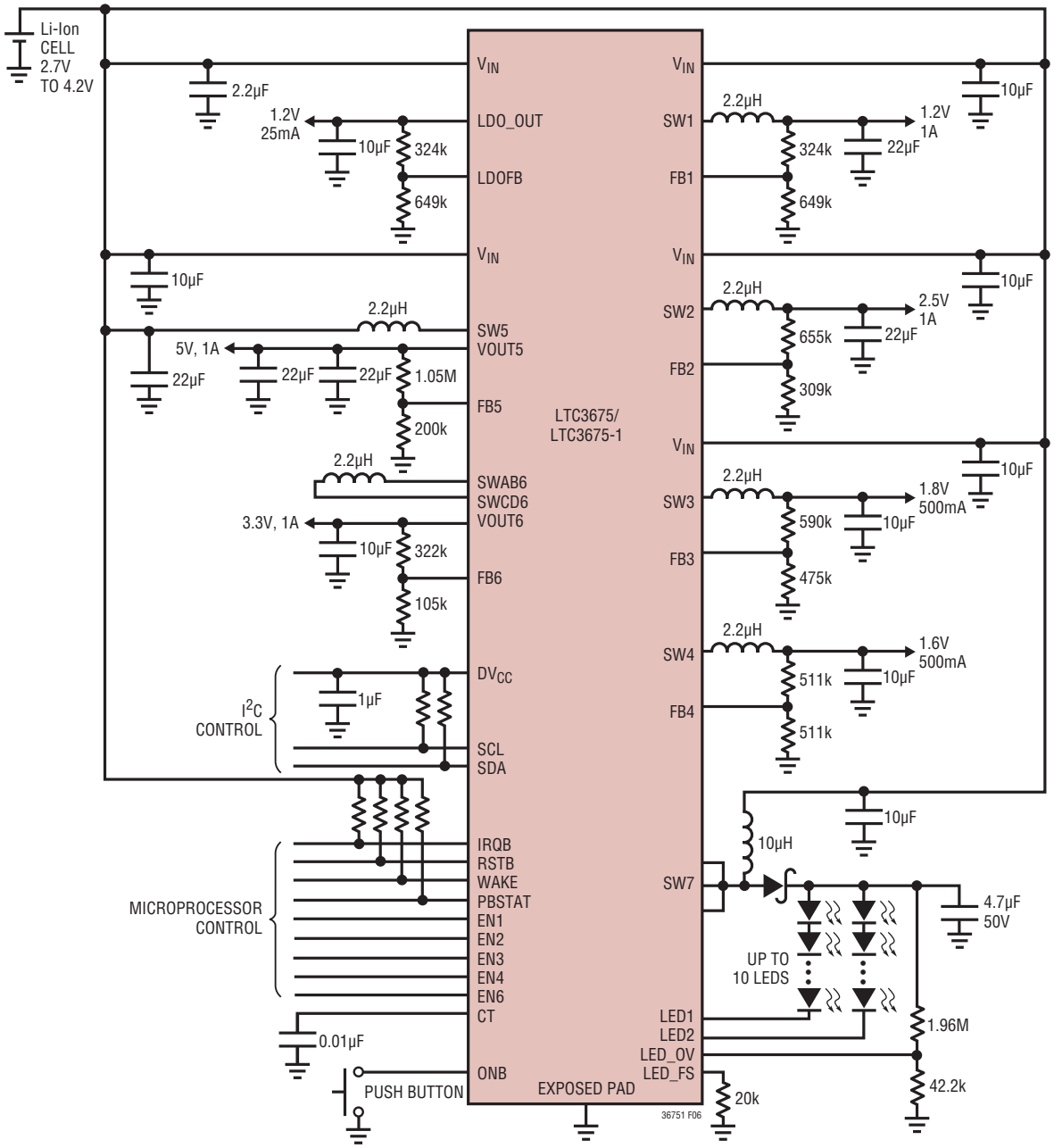


Figure 6. Detailed Front Page Application Circuit

TYPICAL APPLICATIONS

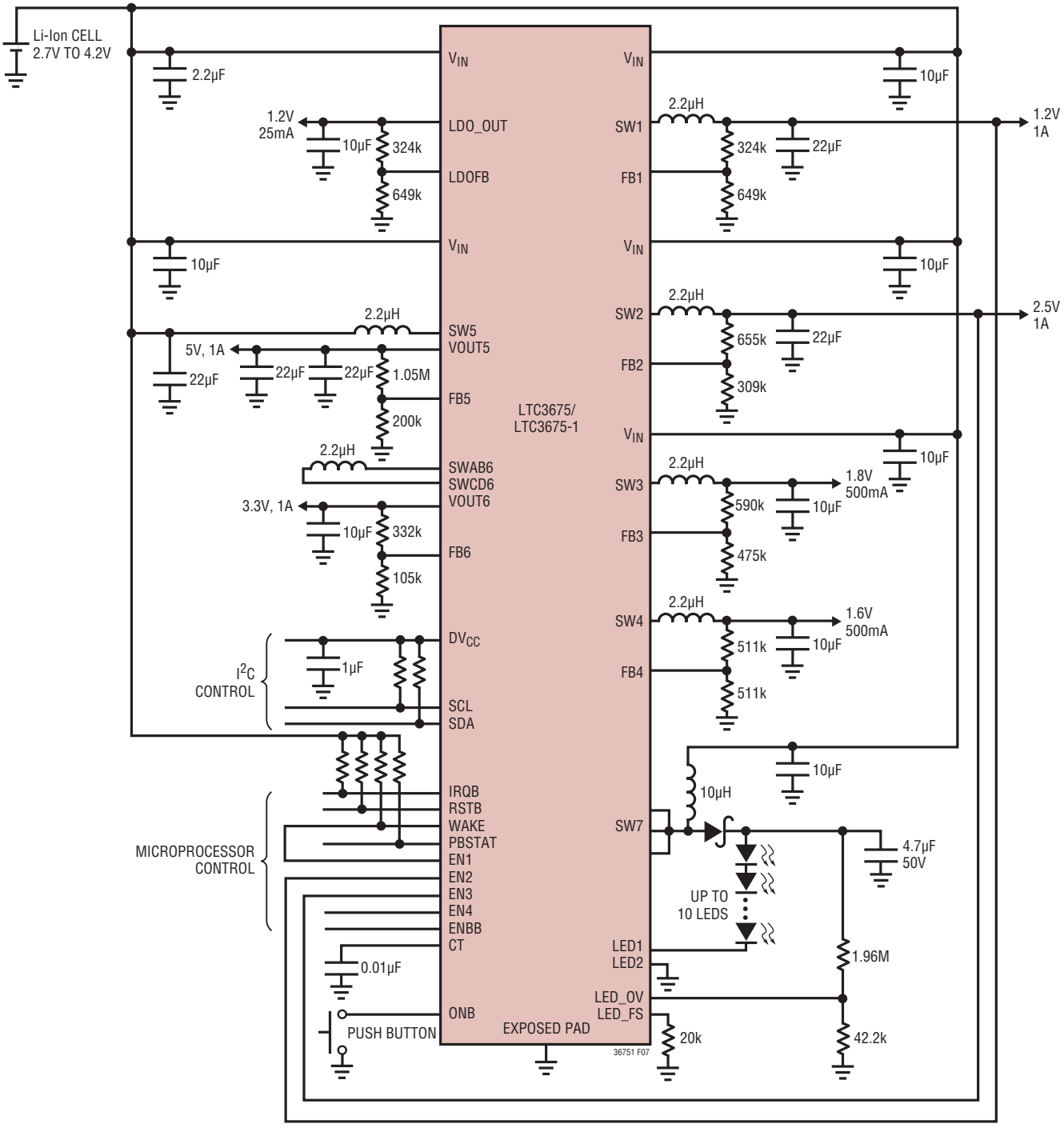


Figure 7. Buck Regulators with Sequenced Start-Up and a Single String of LEDs. Buck Regulators Power-Up in the Sequence Buck1, Buck2 and Buck3

TYPICAL APPLICATIONS

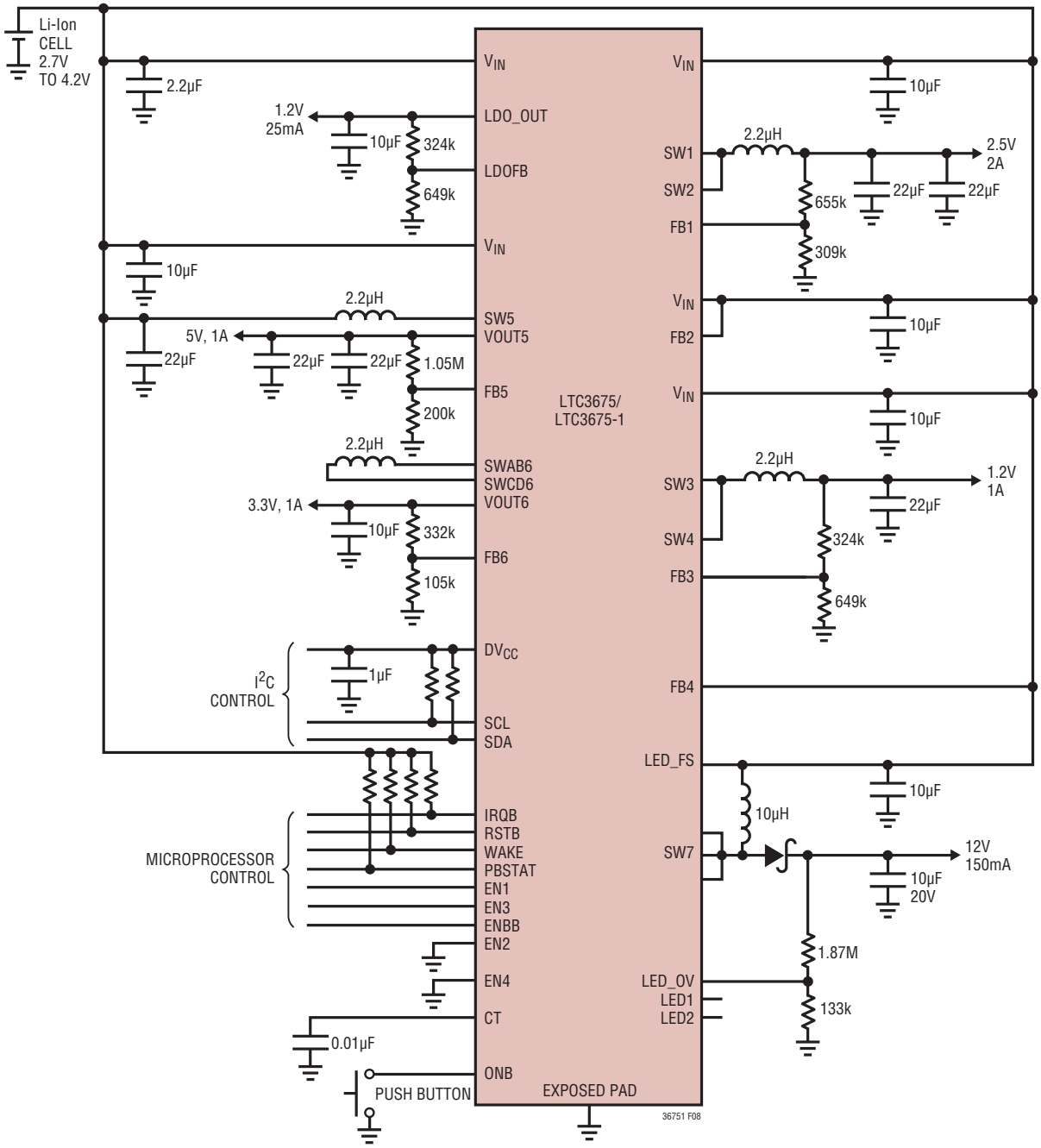
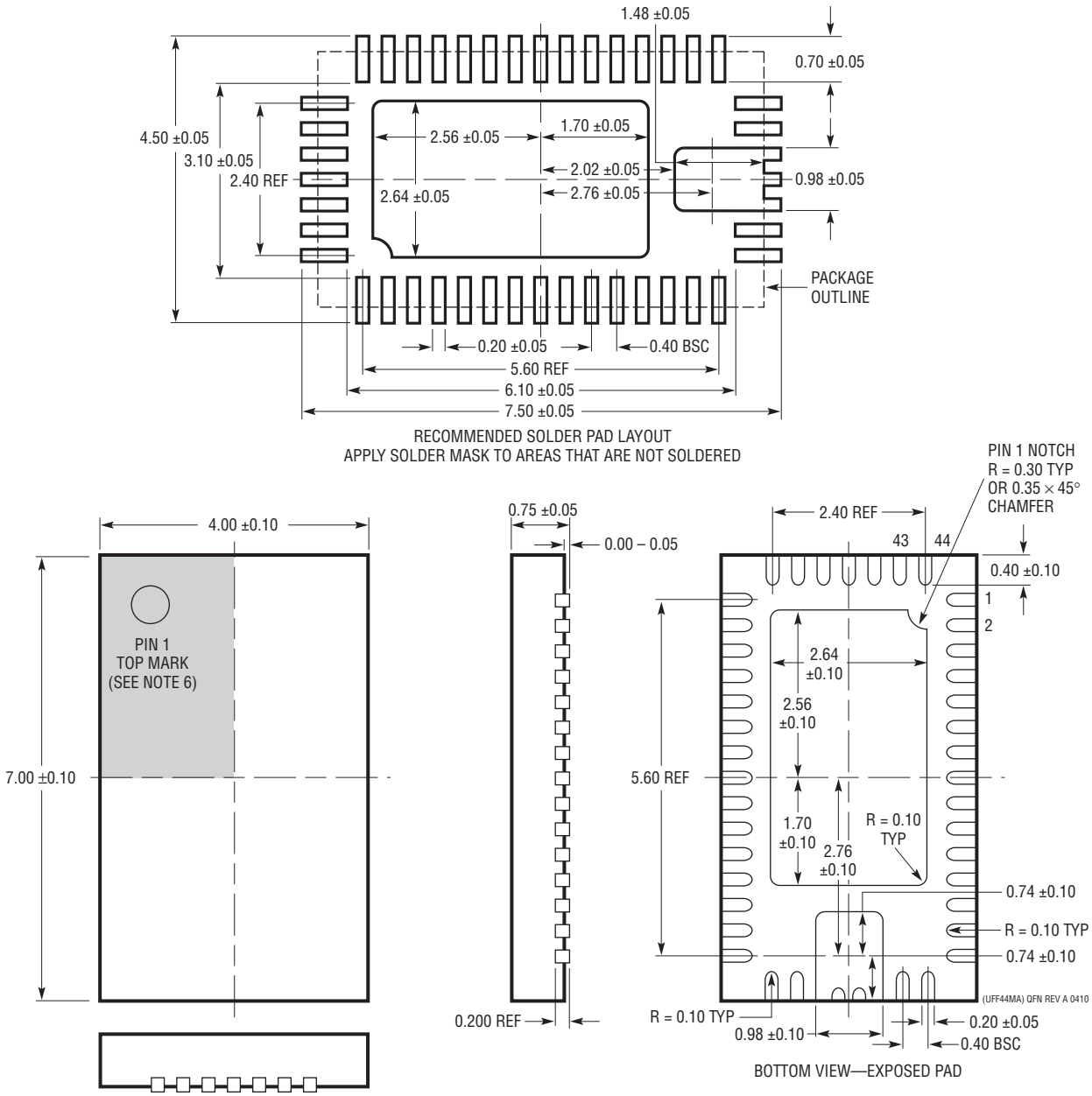


Figure 8. Combined Buck Regulators and a High Voltage Boost Regulator

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFF Package
Variation: UFF44MA
44-Lead Plastic QFN (4mm × 7mm)
(Reference LTC DWG # 05-08-1762 Rev A)

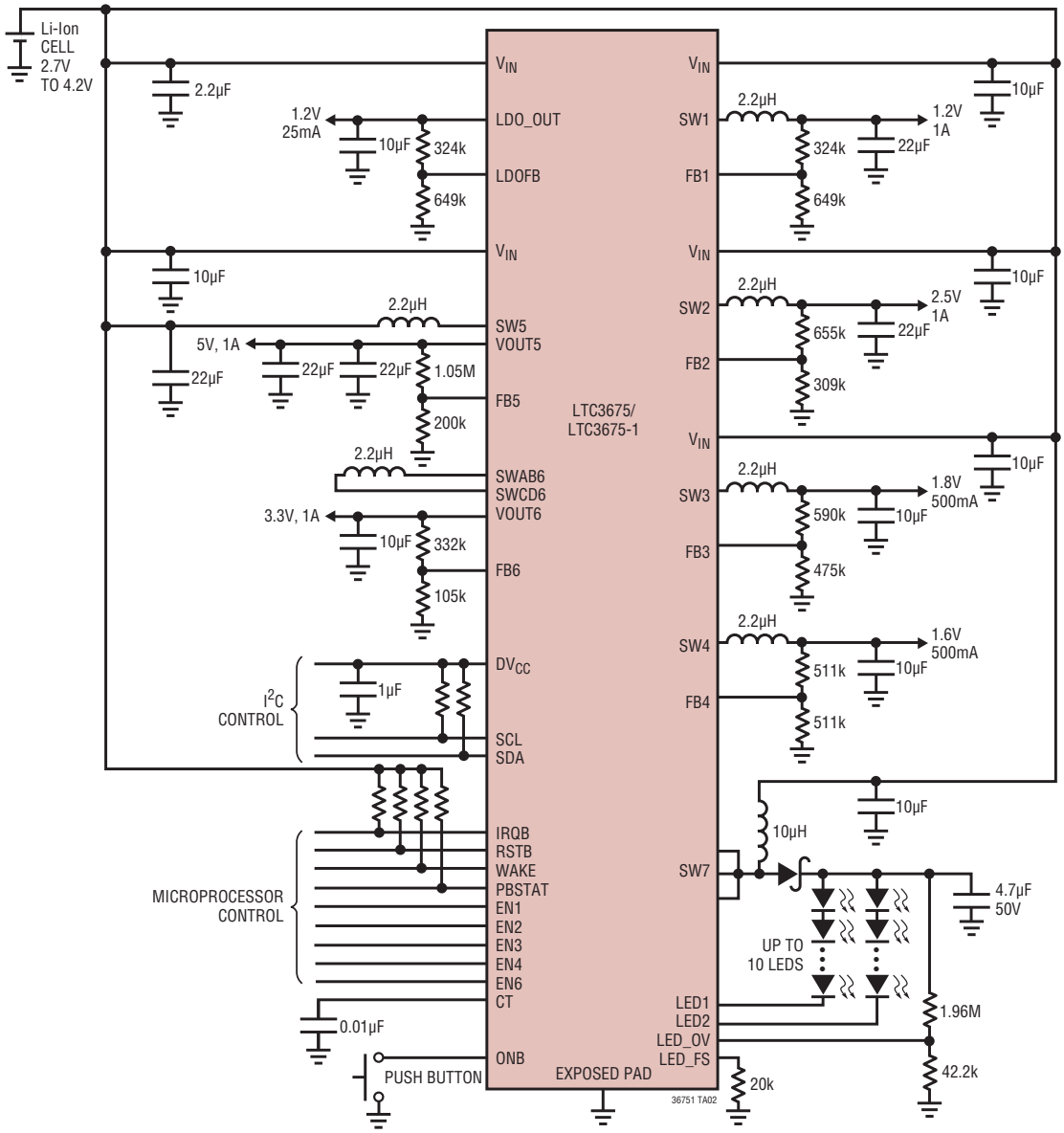


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/12	Clarified PGood Threshold Voltage spec, added Min/Max	4
		Clarified Note 2, electrical grades and temperatures	7
		Modified pin function descriptions for RSTB and IRQB	14
		Changed figure reference in I^2C Interface section	21
		Modified PGood Comparator Polarity Figure 4	24
		Modified Programming the RSTB and IRQB Mask Registers section	30
		Modified Status Byte Read Back section	31
		Modified application circuit V_{IN} caps	33, 34, 35, 38
B	10/12	Added part number LTC3675-1	1 - 38
		Added new I^2C address	6, 21-23
		Clarified maximum ambient temperature in Note 2	7
C	3/13	Clarified EN pin operation	14
		Clarified Buck-Boost EN pin operation	15
		Modified Figure 1 Master-Slave Bucks and Operation	17 to 18
		Modified Figure 8	35

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3569	Triple Buck Regulator with 1.2A and Two 600mA Outputs and Individual Programmable References	Triple, Synchronous, 100% Duty Cycle, PGOOD Pin, Programmable V_{FB} Servo Voltage
LTC3577/ LTC3577-1/ LTC3577-3/ LTC3577-4	Highly Integrated Portable/Navigation PMIC	PMIC: Linear Power Manager and Three Buck Regulators, 10-LED Boost Regulator, Synchronous Bucks ADJ at 800mA/500mA/500mA, PB Control, I^2C Interface, 2× 150mA LDOs, OVP Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation, 4mm × 7mm QFN-44 Package; "-1" and "-4" Versions Have 4.1V V_{FLOAT}, "-3" Version for SiRF Atlas IV Processors
LTC3586/ LTC3586-1	Switching USB Power Manager with Li-Ion/ Polymer Charger, 1A Buck-Boost + Dual Sync Buck Converter + Boost + LDO	PMIC: Switching Power Manager, 1A Buck-Boost + 2 Bucks ADJ to 0.8V at 400mA/400mA + 800mA Boost + LDO, Charge Current Programmable Up to 1.5A from Wall Adapter Input, 4mm × 6mm QFN-38 Package; "-1" Version Has 4.1V V_{FLOAT}