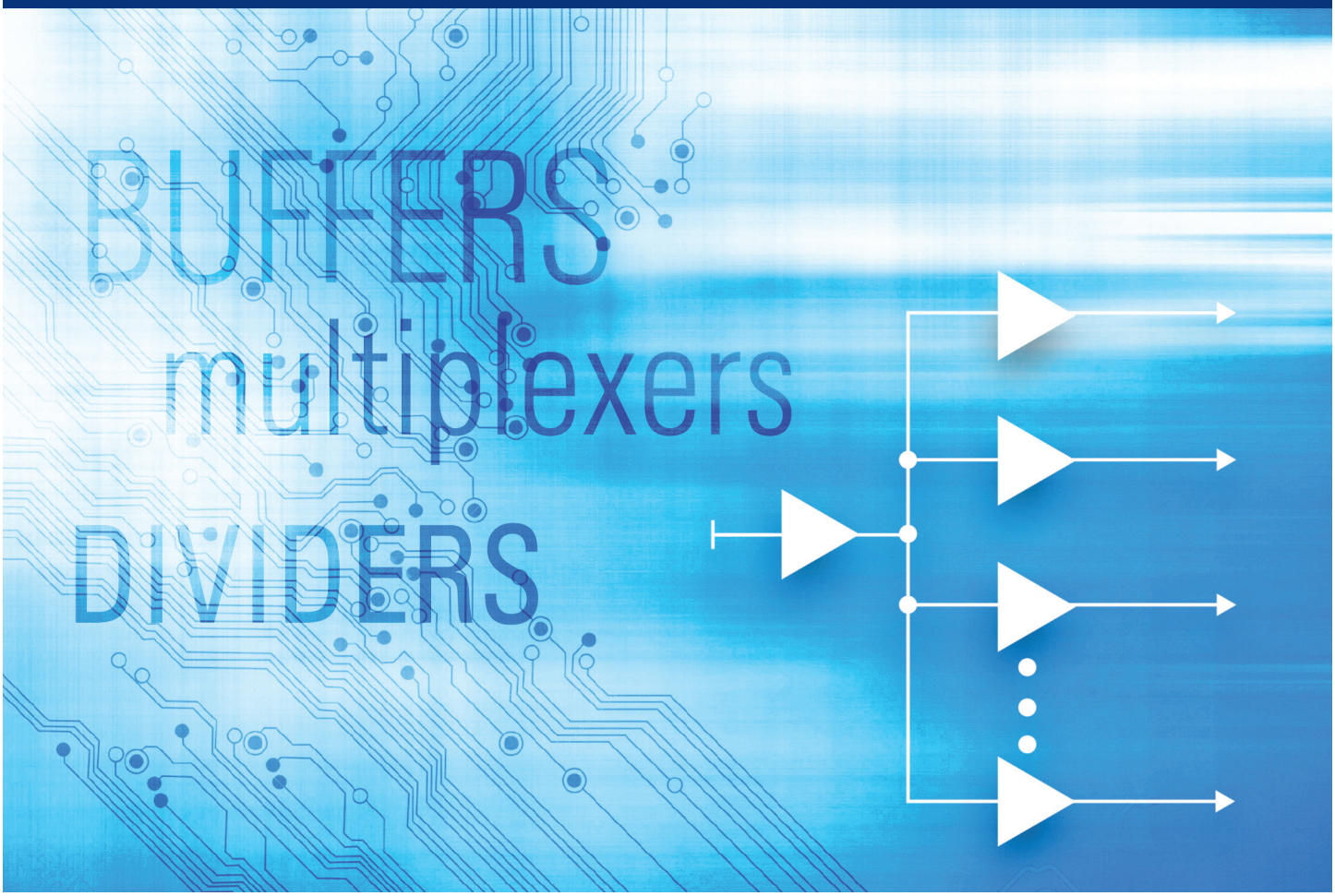
Integrated Device Technology

Clock Distribution Overview



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With a product portfolio 10 times greater and broader than any other, IDT is the world's leader in silicon timing and is in a unique position to address the needs of virtually any application.

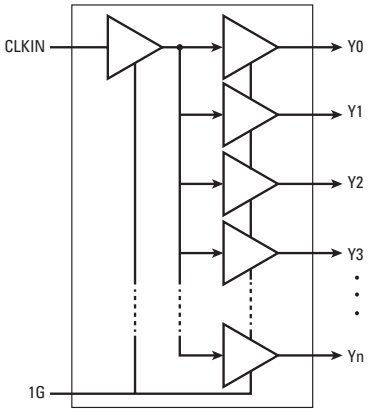
With the industry's largest market share, IDT is the only one-stop-shop for timing, offering products from full-featured system solutions to simple clock building-block devices. Factory-programmable options and clock solution customization capabilities address unique customer requirements, while the lowest jitter and lowest power features set IDT apart from the competition. Products are accompanied by a world-class support team driven by service and responsiveness goals.

The products in this guide represent a portion of IDT's timing portfolio. For more information about IDT's comprehensive portfolio of timing products or to request samples, please visit: **idt.com/go/timing**

FANOUT BUFFERS are a useful building block of many clock trees, providing signal buffering and multiple low-skew copies of the input signal. The clock fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. Single output buffers are useful for translating a clock from one signaling standard to another (e.g. LVCMOS-in to LVPECL-out). Some devices have an integrated crystal oscillator, requiring only a low cost external fundamental-mode quartz crystal. The integrated oscillator provides an extremely low phase noise reference clock to drive jitter sensitive devices such as the clock inputs of PHYs.

ZERO DELAY BUFFERS are ideal for applications requiring synchronized clocking for FPGAs, CPUs, logic and synchronous memory. Zero delay buffers are PLL-based devices that regenerate the input clock signal with fanout to drive multiple loads. Most devices allow the delay through the device to be adjusted through an external feedback path. This allows precise control of the timing of the clock signals to the loads. Zero delay buffers provide a synchronous copy of the input clock at the outputs, usually without frequency translation. Simple frequency translation is possible when a single divider is used for all outputs, including feedback output, to maintain clock synchronization.

LVCMOS Buffers

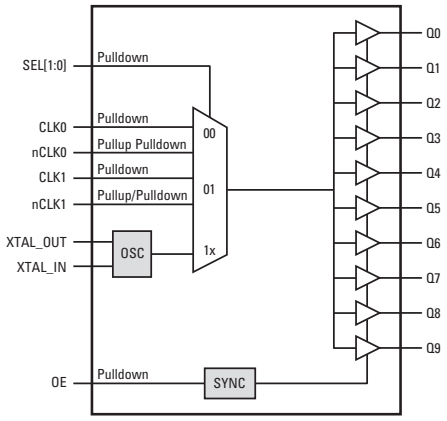


5PB11xx - 1.8V to 3.3V LVCMOS High Performance Clock Buffer

- High performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew <50 ps
- Very low additive jitter <50 fs
- Supply voltage: 1.8 V to 3.3 V
- Packaged in 8-, 14-,16-, 20-TSSOP and small DFN and QFN packages

8L30110 – Crystal or Differential to LVCMOS/LVTTL Clock Buffer

- Up to 10 outputs
- Dual reference inputs or crystal input
- Output power supply modes of 3.3, 2.5, 1.8 or 1.5 volts
- Low output skew, 63 ps (typical)
- Low additive phase jitter, 22 fs (typical)
- 5 x 5 mm 32-VFQFN package

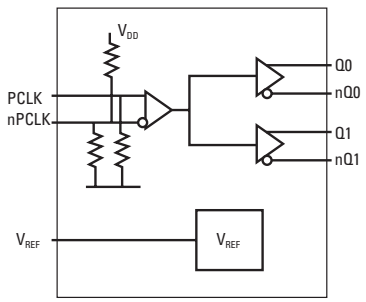


Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
5PB1102	1.8V to 3.3V 1:2 LVCMOS High-Performance Clock Buffer	2	0 - 200	1.8, 2.5, 3.3	65	35
74FCT38072S	Low Skew 1 to 2 Clock Buffer	2	0 - 200	1.8, 2.5, 3.3	65	35
5P1103	Programmable Fanout Buffer	3	1 - 350	1.8, 2.5, 3.3	35	200
524S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
551S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
553S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
5PB1104	1.8V to 3.3V 1:4 LVCMOS High-Performance Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
621S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
651S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35

LVCMOS Buffers, continued

Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
74FCT38074S	Low Skew 1 to 4 Clock Buffer	4	0 - 200	1.8, 2.5, 3.3	65	35
74FCT38075S	Low Skew 1 to 5 Clock Buffer	5	0 - 200	1.8, 2.5, 3.3	65	35
8305i	Low Skew, 1-to-4, Multiplexed Differential / LVCMOS-to-LVCMOS / LVTTL Fanout Buffer	4	0 - 350	1.8, 2.5, 3.3	40	40
8L30205	Crystal or Differential to LVCMOS/LVTTL Clock Buffer	5	0 -200	3.3, 2.5, 1.8, 1.5	55	30
5P1105	Programmable Fanout Buffer	5	1 - 350	1.8, 2.5, 3.3	35	200
5PB1106	1.8V to 3.3V 1:6 LVCMOS High-Performance Clock Buffer	6	0 - 200	1.8, 2.5, 3.3	65	35
5PB1108	1.8V to 3.3V 1:8 LVCMOS High-Performance Clock Buffer	8	0 - 200	1.8, 2.5, 3.3	65	35
8308i	Low Skew, 1-to-8 Differential / LVCMOS-to-LVCMOS Fanout Buffer	8	0 - 350	2.5, 3.3	100	—
8L3010	Crystal or Differential to LVCMOS/LVTTL Clock Buffer	10	0 -200	3.3, 2.5, 1.8, 1.5	50	24
8L30210	Crystal or Differential to LVCMOS/LVTTL Clock Buffer	10	0 -200	3.3, 2.5, 1.8, 1.5	55	30
8L30110	Crystal or Differential to LVCMOS/LVTTL Clock Buffer	10	0 -200	3.3, 2.5, 1.8, 1.5	63	22
5PB1110	1.8V to 3.3V 1:10 LVCMOS High-Performance Clock Buffer	10	0 - 200	1.8, 2.5, 3.3	65	35
74FCT3807S	Low Skew 1 to 10 Clock Buffer	10	0 - 200	1.8, 2.5, 3.3	65	35
8343-01	Low Skew, 1-to-16 LVCMOS / LVTTL Fanout Buffer	16	0 - 200	2.5, 3.3	250	—
83940Di	Low Skew,1-to-18 LVPECL-to-LVCMOS/ LVTTL Fanout Buffer	18	0 - 250	2.5, 3.3	150	—
83918i	Low Skew,1:18 Crystal-to-LVCMOS/ LVTTL Fanout Buffer	18	0 - 200	1.8, 2.5, 3.3	75	145

LVDS Buffers



8P34S1102i - 1:2 LVDS Output 1.8V Fanout Buffer

- Two low skew, low additive jitter LVDS output pairs
- One differential clock input pair
- Differential PCLK, nPCLK pair can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 1.2 GHz
- Low additive RMS phase jitter < 42 fs (typical)
- 3 x 3 mm 16-VFQFN package

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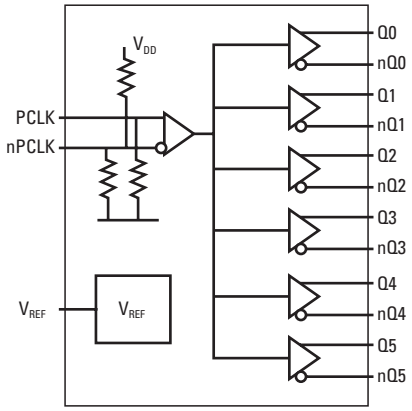
LVDS Buffers, continued

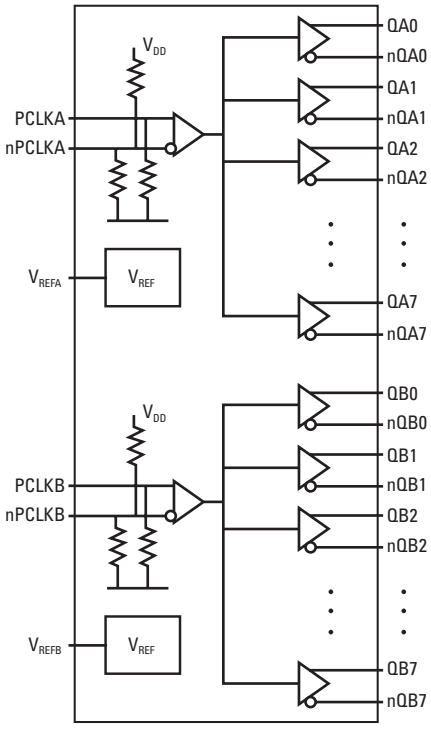


8P34S1106i - 1:6 LVDS Output 1.8V Fanout Buffer

- Six low skew, low additive jitter LVDS output pairs
- One differential clock input pair
- Differential PCLK, nPCLK pair can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 1.2 GHz (maximum), design target
- Low additive RMS phase jitter <39 fs (typical)
- 4 x 4 mm 20-VFQFN package

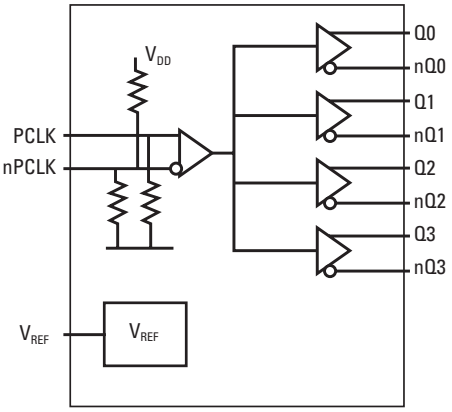
Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Input Type	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
8P34S1102i	1:2 LVDS Output 1.8V Fanout Buffer	2	0 - 1200	LVPECL, LVDS, CML	1.8	20	42
5P1103	Programmable Fanout Buffer	3	1 - 350	LVCMOS, LVPECL, LVDS, HCSL, Crystal	1.8, 2.5, 3.3	35	200
8SLVD1204i	2:4, LVDS Output Fanout Buffer	4	0 - 2000	LVDS, LVPECL	2.5	20	95
8SLVD2102i	Dual 1:2, LVDS Output Fanout Buffer	4	0 - 2000	LVDS, LVPECL	2.5	15	80
8P34S1204i	1:4 LVDS Output 1.8V Fanout Buffer	4	0 - 1200	LVDS, LVPECL, CML	1.8	14	42
8SLVD1204-33	2:4, LVDS Output Fanout Buffer	4	0 - 2000	LVDS, LVPECL	3.3	20	67
5P1105	Programmable Fanout Buffer	5	1 - 350	LVCMOS, LVPECL, LVDS, HCSL, Crystal	1.8, 2.5, 3.3	35	200
8P34S1106i	1:6 LVDS Output 1.8V Fanout Buffer	6	0 - 1200	LVPECL, LVDS, CML	1.8	20	39
8SLVD1208i	2:8, LVDS Output Fanout Buffer	8	0 - 2000	LVDS, LVPECL	2.5	8	65
8SLVD1208-33	2:8, LVDS Output Fanout Buffer	8	0 - 2000	LVDS, LVPECL	3.3	20	82
8SLVD2104	Dual 1:4, LVDS Output Fanout Buffer	8	0 - 2000	LVDS, LVPECL	2.5	20	72
8P34S1208i	1:8 LVDS Output 1.8V Fanout Buffer	8	0 - 1200	LVDS, LVPECL, CML	1.8	20	41
8T39S10i	Crystal or Differential to Differential Clock Fanout Buffer	10	0 - 2000	Crystal, LVPECL, LVDS, HCSL	2.5, 3.3	70	150
8T39S11	Crystal or Differential to Differential Clock Fanout Buffer	10	0 - 2000	LVDS, LVPECL, HCSL, HSTL, LVCMOS	2.5, 3.3	80	176
8SLVD1212	1:12, LVDS Output Fanout Buffer	12	0 - 2000	LVDS, LVPECL, CML	2.5	45	77
8P34S1212i	1:12 LVDS Output 1.8V Fanout Buffer	12	0 - 1200	LVDS, LVPECL, CML	1.8	12	73
8T349316	1:16 LVDS Clock Fanout Buffer	16	0 -1000	LVPECL, HCSL, HSTL, LVTTL	2.5	50	—

LVPECL Buffers



8SLVP1104i - Low Phase Noise, 1-to-4, 3.3V, 2.5V LVPECL Output Fanout Buffer

- Four low skew, low additive jitter LVPECL differential output pairs
- Differential LVPECL input pair can accep the following differential input levels: LVDS, LVPECL, CML
- Differential PCLKx pairs can also accept single-ended LVCMOS levels. LVCMOS interface levels for the control input (input select)
- Low additive RMS phase jitter <40 fs max
- 3 x 3 mm 16-VFQFN



8SLVP2108i - Dual 1:8, 3.3V, 2.5V LVPECL Fanout Buffer

- Two 1:8, low skew, low additive jitter LVPECL fanout buffers
- Two differential clock inputs
- Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels.
- Maximum input clock frequency: 2 GHz
- Low additive RMS phase jitter <54 fs (maximum)
- 7 x 7 mm 48-VFQFN package

Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Output Banks (#)	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
8SLVP1102i	1:2, LVPECL Output Fanout Buffer	2	0 - 2000	1	CML, LVDS, LVPECL	1	2.5, 3.3	15	36
853S011Bi	Low Skew, 1-to-2, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	2	0 - 2500	1	CML, LVDS, LVPECL, SSTL	1	2.5, 3.3	5	26
853S011Ci	Low Skew, 1-to-2, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	2	0 - 2500	1	CML, LVDS, LVPECL, SSTL	1	2.5, 3.3	20	35
5P1103	Programmable Fanout Buffer	3	1 - 350	2	LVCMOS, LVPECL, LVDS, HCSL, Crystal	1	1.8, 2.5, 3.3	35	200
8SLVP1104i	Low Phase Noise, 1-to-4, 3.3V, 2.5V LVPECL Output Fanout Buffer	4	0 - 2000	1	CML, LVDS, LVPECL	1	2.5, 3.3	15	32
8SLVP2102i	Dual 1:2, 3.3V, 2.5V LVPECL Output Fanout Buffer	4	0 - 2000	2	CML, LVDS, LVPECL	2	2.5, 3.3	15	31
8S89831i	Differential LVPECL-to-LVPECL/ECL Fanout Buffer	4	0 - 2100	1	CML, LVDS, LVPECL, SSTL	1	3.3	30	310

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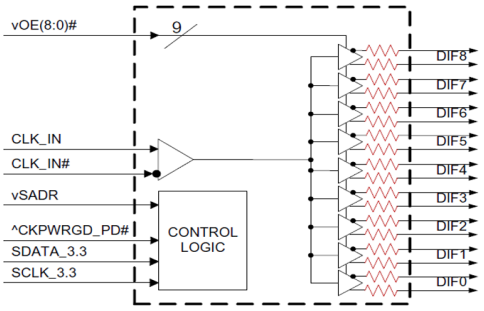
LVPECL Buffers, continued

Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Output Banks (#)	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
8SLVP1204i	2:4, LVPECL Output Fanout Buffer	4	0 - 2000	2	LVDS, LVPECL, CML	1	2.5, 3.3	40	5
5P1105	Programmable Fanout Buffer	5	1 - 350	2	LVCMOS, LVPECL, LVDS, HCSL, Crystal	1	1.8, 2.5, 3.3	35	200
853S006i	Low Skew, 1-to-6, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	6	0 - 2000	2	CML, LVDS, LVPECL	1	2.5, 3.3	50	100
853S013i	Low Skew,Dual, 1-to-3, Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	6	0 - 2000	2	CML, LVDS, LVPECL, SSTL	2	2.5, 3.3	60	50
8SLVP2104i	Dual 1:4, 3.3V, 2.5V LVPECL Output Fanout Buffer	8	0 - 2000	2	CML, LVDS, LVPECL	2	2.5, 3.3	25	43
853S310i	Low Skew, 1-to-8 Differential-to-3.3V LVPECL/ECL Fanout Buffer	8	0 -2000	1	LVPECL, LVDS, CML, SSTL	1	3.0V to 3.8V	140	20
8SLVP1208i	2:8, LVPECL Output Fanout Buffer	8	0 - 2000	2	LVDS, LVPECL, CML	1	2.5, 3.3	54	28
8T53S111i	1:10 LVPECL Output Fanout Buffer	10	0 - 2500	1	LVDS, LVPECL	1	2.5, 3.3	30	15
8T33FS6111	Low Voltage 2.5V/3.3V Differential LVPECL / HSTL Fanout Buffer	10	0 - 2700	2	LVPECL, HSTL	1	2.5, 3.3	50	100
8T39S10i	Crystal or Differential to Differential Clock Fanout Buffer	10	0 - 2000	3	Crystal, LVPECL, LVDS, HCSL	2	2.5, 3.3	70	150
8T39S11	Crystal or Differential to Differential Clock Fanout Buffer	10	0 - 2000	3	Xtal, LVPECL, LVDS, HCSL, HSTL, LVCMOS	2	2.5, 3.3	80	35
853S12i	Low Skew,1-to-12, Differential-to-3.3V, 2.5V LVPECL Fanout Buffer	12	0 - 1500	1	CML, LVPECL, SSTL	1	2.5, 3.3	50	60
8SLVP2106i	Dual 1:6, 3.3V, 2.5V LVPECL Output Fanout Buffer	12	0 - 2000	2	LVDS, LVPECL	2	2.5, 3.3	26	42
8T33FS6222	Low Voltage, 1:15 Differential PECL Clock Divider and Fanout Buffer	15	0 - 750	2	LVPECL	4	2.5, 3.3	31.25	127
8SLVP2108i	Dual 1:8, 3.3V, 2.5V LVPECL Output Fanout Buffer	16	0 - 2000	2	LVPECL	2	2.5, 3.3	25	43
8530i-01	Low Skew, 1-to-16 Differential-to-3.3V LVPECL Fanout Buffer	16	0 - 500	1	LVPECL, LVDS, LVHSTL, HCSL, SSTL	1	3.3	162	75
8T33FS6221	Low Voltage 1:20 Differential PECL/HSTL Clock Fanout Buffer	20	0 - 2000	2	PECL, HSTL	1	2.5, 3.3	78	50

HCSL Fanout Buffers

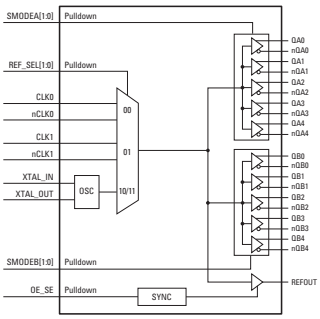


9DBV0941: 9-output 1.8 V PCIe® Gen1/2/3 Fanout Buffer with Zo = 100 Ω

- Additive phase jitter is <100 fs RMS for PCIe Gen3
- Additive phase jitter is <300 fs RMS (12 k to 20 M)
- Push-pull LP-HCSL outputs with integrated terminations save 36 resistors compared to standard HCSL
- 56 mW typical power consumption eliminates thermal concerns
- 1 MHz to 200 MHz operating frequency supports other interfaces such as Ethernet
- Space-saving 6 x 6 mm VFQFPN-48

Product ID	Product Title	Outputs (#)	Diff. Output Signaling	Output Frequency Range	Diff. Inputs	Input Type	Supply Voltage (V)	Supply Output Supply Voltage
9DBU0541	5-output 1.5 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	5	LP-HCSL	1-167	1	HCSL	1.5	1.5
9DBV0541	5-output 1.8 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	5	LP-HCSL	1-200	1	HCSL	1.8	1.05 - 1.8
9DBU0741	7-output 1.5 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	7	LP-HCSL	1-167	1	HCSL	1.5	1.05 - 1.5
9DBV0741	7-output 1.8 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	7	LP-HCSL	1-200	1	HCSL	1.8	1.05 - 1.8
9DBU0941	9-output 1.5 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	9	LP-HCSL	1-167	1	HCSL	1.5	1.05 - 1.5
9DBV0941	9-output 1.8 V PCIe Gen1/2/3 Fanout Buffer with Zo=100 Ω	9	LP-HCSL	1-200	1	HCSL	1.8	1.05 - 1.8

Universal Output Buffers

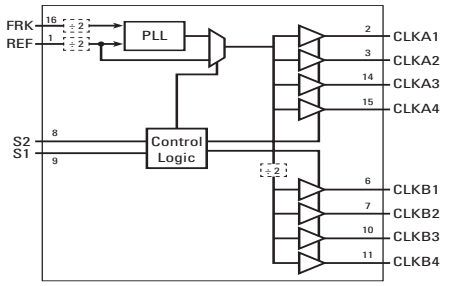


8T39S11 - Crystal or Differential to Differential Clock Fanout Buffer

- 10 total outputs with 2 banks (5 outputs each)
- Dual reference inputs or crystal input
- Selectable output levels: LVPECL, LVDS, HCSL and LVCMOS
- Up to 2 GHz operation for LVPECL and LVDS outputs
- Low output skew, 80 ps max
- Low additive phase jitter, 34.7 fs (typical)
- 7 x 7 mm 48-VFQFN package

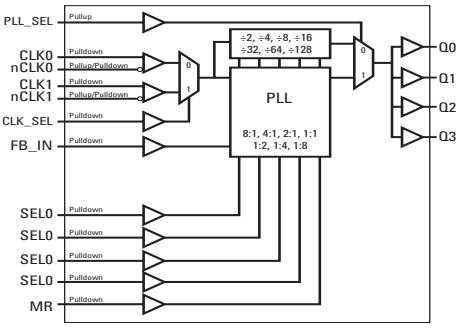
Product ID	Product Title	Outputs (#)	Output Type	Output Freq Range (MHz)	Input Freq (MHz)	Inputs (#)	Input Type	Core Voltage (V)	Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
5P1103	Programmable Fanout Buffer	3	HCSL, LVCMOS, LVDS, LVPECL	1 - 350	1 - 350	2	Crystal, HCSL, LVCMOS, LVDS, LVPECL	1.8, 2.5, 3.3	1.8, 2.5, 3.3	35	200
5P1105	Programmable Fanout Buffer	5	HCSL, LVCMOS, LVDS, LVPECL	1 - 350	1 - 350	2	Crystal, HCSL, LVCMOS, LVDS, LVPECL	1.8, 2.5, 3.3	1.8, 2.5, 3.3	35	200
8T39S10i	Crystal or Differential to Differential Clock Fanout Buffer	11	HCSL, LVCMOS, LVDS, LVPECL	0 - 500	0 - 500	3	Crystal, HCSL, LVDS, LVPECL	2.5, 3.3	2.5, 3.3	32	185
8T39S11	Crystal or Differential to Differential Clock Fanout Buffer	10	HCSL, LVCMOS, LVDS, LVPECL	0 - 2000	0 - 250	3	Xtal, LVPECL, LVDS, HCSL, HSTL, LVCMOS	2.5, 3.3	2.5, 3.3	35	26

LVCMOS Zero Delay Buffers



2308B - 3.3V Zero Delay Clock Multiplier

- Phase-lock loop clock distribution for applications ranging from 10 MHz to 133 MHz operating frequency
- Distributes one clock input to two banks of four outputs
- Separate output enable for each output bank
- External feedback (FBK) pin is used to synchronize the outputs to the clock input
- 9.9 x 3.9 mm 16-SOIC and 5 x 4.4 mm 16-TSSOP packages



87004i - 1:4, Differential-to-LVCMOS/LVTTL Zero Delay Clock Generator

- Four LVCMOS/LVTTL outputs, 7 Ω typical output impedance
- Selectable CLK0/nCLK0 or CLK1/nCLK1 clock inputs
- CLKx/nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Internal bias on nCLK0 and nCLK1 to support LVCMOS/LVTTL levels on CLK0 and CLK1 inputs
- Output frequency range: 15.625 MHz to 250 MHz
- 7.8 x 4.4 mm 24-TSSOP package

Product ID	Product Title	Outputs (#)	Freq Range (MHz)	Inputs (#)	Input Type	Output Banks (#)	Supply, Output Voltage (V)
527-01	Clock Slicer User Configurable Zero Delay Buffer	2	4 - 160	1	LVCMOS	2	3.3
570	Multiplier and Zero Delay Buffer	2	10 - 170	1	LVCMOS	1	3.3, 5
571	Low Phase Noise Zero Delay Buffer	2	10 - 160	1	LVCMOS	2	3.3, 5
670-01	Low Phase Noise Zero Delay Buffer	2	24 - 160	1	LVCMOS	2	3.3, 5
670-03	Low Phase Noise Zero Delay Buffer	2	24 - 210	1	LVCMOS	2	3.3, 5
87002-02	1:2, Differential-to-LVCMOS/LVTTL Zero Delay Clock Generator	2	15.625 - 250	1	HCSL, HSTL, LVDS, LVPECL, SSTL	1	2.5, 3.3
87002-05	1:2 LVCMOS/LVTTL-to-LVCMOS / LVTTL Zero Delay Buffer For Audio	2	11.2783 - 24.6005	1	LVCMOS	1	3.3
574	Zero Delay, Low Skew Buffer	4	20 - 160	1	LVCMOS	1	3.3, 5
86004	15.625 MHZ TO 62.5 MHZ, 1:4 LVCMOS/LVTTL Zero Delay Buffer	4	15.625 - 62.5	1	LVCMOS	1	2.5, 3.3
86004i	15.625 MHz to 62.5 MHz, 1:4 LVCMOS/ LVTTL Zero Delay Buffer	4	15.625 - 62.5	1	LVCMOS	1	2.5, 3.3

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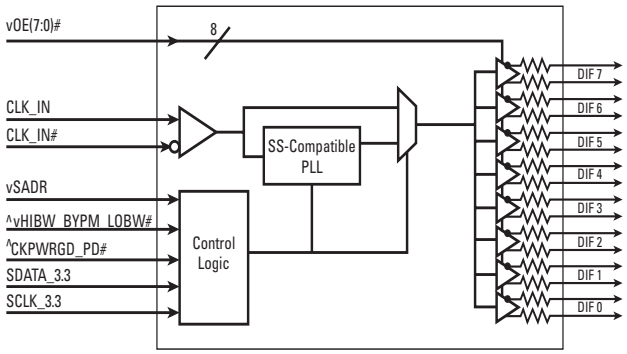
LVCMOS Zero Delay Buffers, continued

Product ID	Product Title	Outputs (#)	Freq Range (MHz)	Inputs (#)	Input Type	Output Banks (#)	Supply, Output Voltage (V)
87004i	1:4, Differential-to-LVCMOS/LVTTL Zero Delay Clock Generator	4	15.625 - 250	2	HCSL, HSTL, LVDS, LVPECL, SSTL	1	2.5, 3.3
2308B	3.3V Zero Delay Clock Multiplexer	8	10 - 133.3	1	LVCMOS	2	3.3
8705i	Zero Delay, Differential-to-LVCMOS/LVTTL Clock Generator	8	15.625 - 250	2	HCSL, HSTL, LVCMOS, LVDS, LVPECL, SSTL	1	2.5, 3.3
87972i-147	Low Skew, 1-to-12 LVCMOS/LVTTL Clock Multiplier/Zero Delay Buffer	13	10 - 150	3	Crystal, LVCMOS	4	3.3
87973i-147	Low Skew, 1-to-12 LVCMOS/LVTTL Clock Multiplier/Zero Delay Buffer	13	10 - 150	3	HCSL, HSTL, LVCMOS, LVDS, LVPECL, SSTL	4	3.3

HCSL Zero Delay Buffers



9DBV0841 1.8V 8-output PCIe Gen 1/2/3 Zero Delay/Fan out Buffer with Zo=100 Ω

- Additive phase jitter is 100 fs rms typical for PCIe Gen3 (bypass mode)
- Additive phase jitter is 250 fs rms typical (12 k-20 M, bypass mode)
- 1 MHz to 200 MHz operating frequency (bypass mode)
- Direct connection to 100 transmission lines; saves 32 resistors compared to standard HCSL outputs
- 64 mW (typical) power consumption eliminates thermal concerns
- 6 x 6 mm 48-VFQFPN

Product ID	Product Title	Outputs (#)	Output Type	Output Freq Range (MHz)	Inputs (#)	Input Type	Supply Voltage (V)	Supply, Output Supply Voltage (V)
9DBU0241	2-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	2	LP-HCSL	1-167	1	HCSL	1.5	1.5
9DBV0241	2-output 1.8 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	2	LP-HCSL	1-200	1	HCSL	1.8	1.8
8714004i	FemtoClock® Zero Delay Buffer/Clock Generator for PCIe and Ethernet	4	HCSL	98 - 165	2	LVPECL, LVDS, M-LVDS, LVHSTL, HCSL	3.3	3.3
9DBU0431	4-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer	4	LP-HCSL	1-167	1	HCSL	1.5	1.5
9DBU0441	4-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	4	LP-HCSL	1-167	1	HCSL	1.5	1.5

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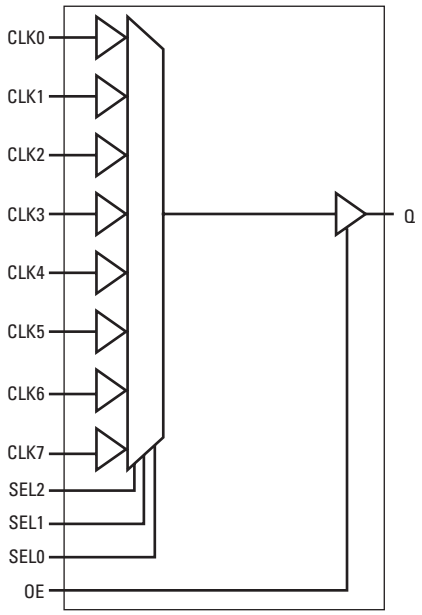
HCSL Zero Delay Buffers, continued

Product ID	Product Title	Outputs (#)	Output Type	Output Freq Range (MHz)	Inputs (#)	Input Type	Supply Voltage (V)	Supply, Output Supply Voltage (V)
9DBV0441	4-output 1.8 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	4	LP-HCSL	0-200	1	HCSL	1.8	1.8
9ZXL0651	DB600ZL Derivative with Zo = 85 Ω	6	LP-HCSL	33-150	1	HCSL	3.3	3.3
9DBU0631	6-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer	6	LP-HCSL	0-167	1	HCSL	1.5	1.05-1.5
9DBU0641	6-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	6	LP-HCSL	1-167	1	HCSL	1.5	1.05-1.5
9DBV0641	6-output 1.8 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	6	LP-HCSL	0-200	1	HCSL	1.8	1.05-1.8
9ZXL0831	DB800ZL	8	LP-HCSL	33-150	1	HCSL	3.3	3.3
9ZXL1251	DB1200ZL Derivative with Zo = 85 Ω	8	LP-HCSL	33-150	1	HCSL	3.3	3.3
8714008i	FemtoClock® Zero Delay Buffer/Clock Generator for PCIe and Ethernet	8	HCSL	98 - 165	2	LVPECL, LVDS, M-LVDS, LVHSTL, HCSL	3.3	3.3
9DBU0841	8-output 1.5 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	8	LP-HCSL	0-167	1	HCSL	1.5	1.05-1.5
9DBV0841	8-output 1.8 V PCIe Gen 1/2/3 Zero Delay / Fanout Buffer with Zo=100 Ω	8	LP-HCSL	0-200	1	HCSL	1.8	1.05-1.8
9ZX21200	12-Output DB1200Z Derivative	12	HCSL	33 - 150	1	HCSL	3.3	3.3
9ZX21201	12-Output DB1200Z Compliant Buffer	12	HCSL	33 - 150	1	HCSL	3.3	3.3
9ZXL1231	12-Output DB1200ZL	12	LP-HCSL	33 - 150	1	HCSL	3.3	1.05-3.3
9ZML1232	2:12 DB1200ZL Derivative	12	LP-HCSL	33-150	2	HCSL	3.3	1.05-3.3
9ZX21501	15-Output DB1900Z Derivative	15	HCSL	33 - 150	1	HCSL	3.3	3.3
9ZXL1530	15-Output DB1900Z Low-Power Derivative	15	LP-HCSL	33 - 150	1	HCSL	3.3	1.05-3.3
9ZXL1550	15-Output DB1900Z Low-Power Derivative with Zo=100 Ω	15	LP-HCSL	33 - 150	1	HCSL	3.3	1.05-3.3
9ZX21901	19-Output DB1900Z Compliant Buffer	19	HCSL	33 - 150	1	HCSL	3.3	3.3
9ZXL1930	19-Output DB1900Z Low-Power Derivative	19	LP-HCSL	33 - 150	1	HCSL	3.3	1.05-3.3
9ZXL1950	19-Output DB1900Z Low-Power Derivative with Zo=100 Ω	19	LP-HCSL	33 - 150	1	HCSL	3.3	1.05-3.3

IDT MULTIPLEXERS allow the selection from multiple clock inputs to drive the output. Devices are available with fanout capability, providing multiple copies of the output signal. Some devices have integrated crystal oscillators, requiring only low cost external fundamental-mode quartz crystals. The integrated oscillators provide an extremely low phase noise reference clock to drive jitter sensitive devices such as the clock inputs of PHYs. Others are available that can translate the input clock from one signaling level to another (e.g. LVCMOS-in to LVPECL-out). Many of IDT's multiplexers feature fully differential internal architecture, even devices with single ended I/Os. This improves jitter due to inherent common-mode noise rejection and improves output skew. The differential circuitry is constant current and therefore injects less noise into system power supplies than single-ended solutions, reducing noise and decreasing EMI compliance concerns.

LVCMOS Multiplexers

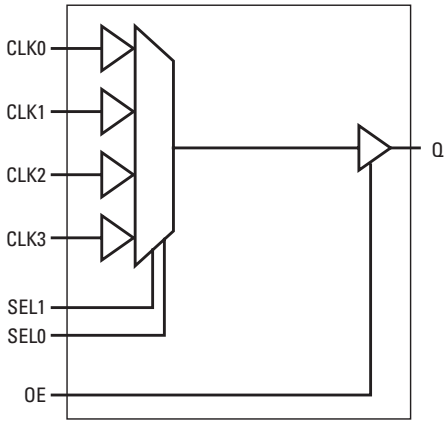


83054i- 4:1 Single-Ended Multiplexer

- 4:1 single-ended multiplexer
- Q nominal output impedance: 7 Ω (VDDO = 3.3 V)
- Maximum output frequency: 250 MHz
- Propagation delay: 3 ns (maximum), VDD = VDDO = 3.3 V
- Additive RMS phase jitter: 140 fs typical
- 4.4 x 5.0 mm 16-TSSOP

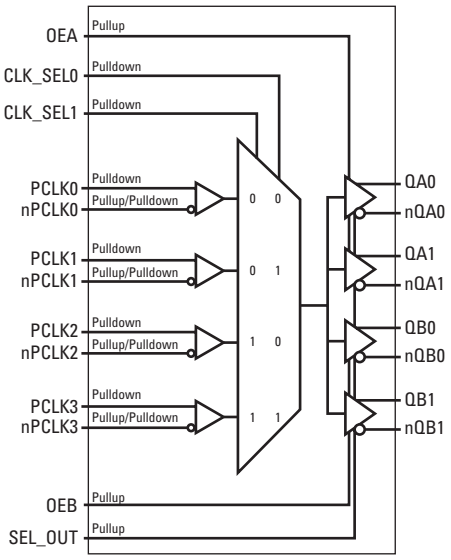
83058i - 8:1 Single-Ended Multiplexer

- 8:1 single-ended multiplexer
- Q nominal output impedance: 7 Ω (VDDO = 3.3 V)
- Maximum output frequency: 250 MHz
- Propagation delay: 3 ns (maximum), VDD = VDDO = 3.3 V
- Additive RMS phase jitter: 140 fs (typical)
- 4.4 x 5 mm 16-TSSOP



Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Core Voltage (V)	Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
83054i	4:1 Single-Ended Multiplexer	1	0 - 250	4	LVCMOS	2.5, 3.3	1.8, 2.5, 3.3	—	140
83056i	6:1 Single-Ended Multiplexer	1	0 - 250	6	LVCMOS	2.5, 3.3	1.8, 2.5, 3.3	—	140
83058i	8:1 Single-Ended Multiplexer	1	0 - 250	8	LVCMOS	2.5, 3.3	1.8, 2.5, 3.3	—	140
850S1201i	12:1 Single-Ended Multiplexer	1	0 - 250	12	LVCMOS	2.5, 3.3	2.5, 3.3	—	35
850S1601i	16:1 Single-Ended Multiplexer	1	0 - 250	16	LVCMOS	2.5, 3.3	2.5, 3.3	—	32
870S208	Differential-to-LVCMOS/ LVTTL Fanout Buffer with Divider and Glitchless Switch	8	0 - 250	2	HCSL, HSTL, LVDS, LVPECL, SSTL	2.5, 3.3	2.5, 3.3	50	—

LVDS Multiplexers

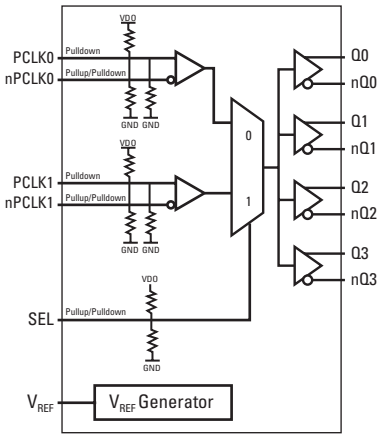


859S0424i - 4:4 Differential-to-LVPECL/LVDS Clock Multiplexer

- High speed 4:1 differential multiplexer with a 1:4 fanout buffer
- Four programmable differential LVPECL or LVDS output pairs
- Four selectable differential PCLKx, nPCLKx input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3 GHz
- 4.4 x 7.8 mm 24-TSSOP package

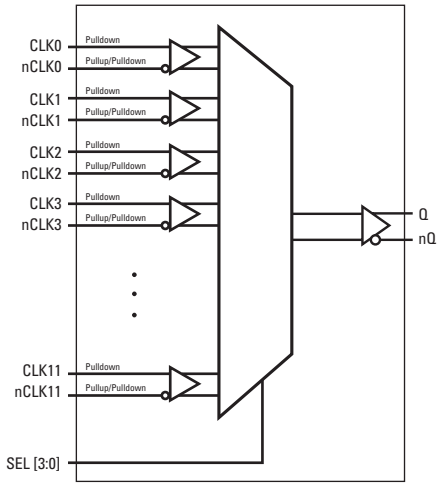
8SLVD1204-33i - 2:4, LVDS Output Fanout Buffer, 3.3 V

- Four low skew, low additive jitter LVDS output pairs
- Two selectable differential clock input pairs
- Differential PCLKx, nPCLKx pairs can accept the following differential input levels: LVDS, LVPECL
- Maximum input clock frequency: 2 GHz
- Low additive RMS phase jitter: 100 fs (maximum)
- 3 x 3 mm 16-VFQFN package



Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
854S01i	2:1 Differential-to-LVDS Multiplexer	1	0 - 2500	2	LVPECL, LVDS	3.3	—	60
854S054i	4:1 Differential-to-LVDS Clock Multiplexer	1	0 - 2500	4	LVPECL, LVDS, CML	3.135	—	147
854S057Bi	4:1 Or 2:1 LVDS Clock Multiplexer with Internal Input Termination	1	0 - 2000	4	CML, LVDS, LVPECL, SSTL	2.5	—	65
854S058i	8:1 Differential-to-LVDS Clock Multiplexer	1	0 - 2500	8	LVDS, LVPECL, SSTL	3.3	—	65
859S0212i	2:2 Differential-to-LVPECL/LVDS Clock Multiplexer	2	0 - 3000	2	CML, LVDS, LVPECL, SSTL	2.5, 3.3	25	21
859S0412i	4:2 Differential-to-LVPECL/LVDS Clock Multiplexer	2	0 - 3000	4	CML, LVDS, LVPECL, SSTL	2.5, 3.3	25	22
859S0424i	4:4 Differential-to-LVPECL/LVDS Clock Multiplexer	4	0 - 3000	4	CML, LVDS, LVPECL	2.5, 3.3	25	22
8P34S1204i	1:4 LVDS Output 1.8V Fanout Buffer	4	0 - 1200	2	LVPECL, LVDS, CML	1.8	14	42
8SLVD1204-33i	2:4, LVDS Output Fanout Buffer, 3.3 V	4	0 - 2000	2	LVPECL, LVDS	3.3	20	95
8SLVD1204i	2:4, LVDS Output Fanout Buffer, 2.5V	4	0 - 2000	2	LVPECL, LVDS	2.5	20	95
854S1208i	Differential-to-LVDS Fanout Buffer with Divider and Glitchless Switch	8	0 - 1500	2	HCSL, LVDS, LVPECL	2.5, 3.3	40	—
8P34S1208i	1:8 LVDS Output 1.8V Fanout Buffer	8	0 - 1200	2	LVPECL, LVDS, CML	1.8	20	41
8SLVD1208-33i	1:8, LVDS Output Fanout Buffer	8	0 - 2000	2	LVPECL, LVDS	3.3	20	82
8SLVD1208i	1:8, LVDS Output Fanout Buffer	8	0 - 2000	2	LVPECL, LVDS	2.5	20	65
8P34S1212i	1:12 LVDS Output 1.8V Fanout Buffer	12	0 - 1200	2	LVPECL, LVDS, CML	1.8	12	73
8SLVD1212	1:12, LVDS Output Fanout Buffer	12	0 - 2000	2	LVPECL, LVDS, CML	2.5	45	65

LVPECL Multiplexers

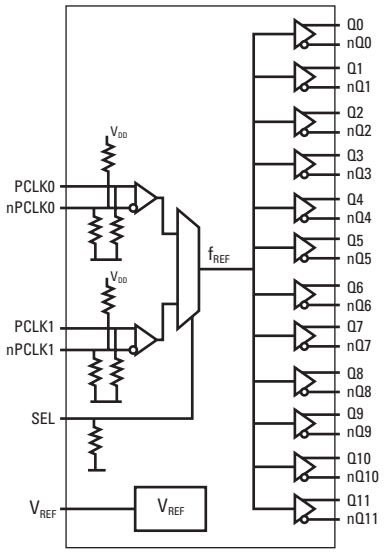


853S012i - 12:1 Differential-to-3.3V, 2.5V LVPECL Clock/Data Multiplexer

- High speed 12:1 differential multiplexer
- One differential 3.3V or 2.5V LVPECL output
- Twelve selectable differential clock or data inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Additive RMS phase jitter: 0.144 ps (typical)
- 5 x 5 mm 32-VFQFN package

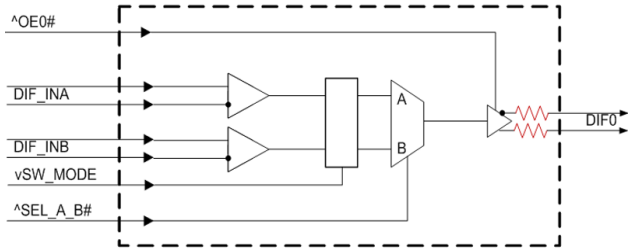
8SLVP1212i - 2:12, 3.3V, 2.5V LVPECL Fanout Buffer

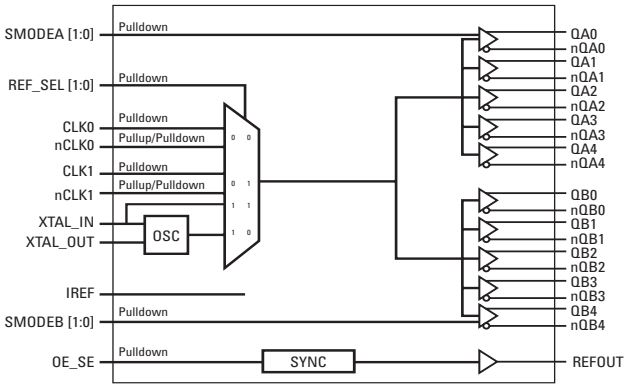
- Twelve low skew, low additive jitter LVPECL outputs
- Two selectable, differential clock inputs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 2 GHz
- Low additive RMS phase jitter: <50 fs (typical)
- 6 x 6 mm 40-VFQFN package



Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
853S012i	12:1 Differential-to-3.3V, 2.5V LVPECL Clock/Data Multiplexer	1	0 - 3200	12	CML, LVDS, LVPECL	2.5, 3.3	—	144
853S01i	2:1 Differential-to-LVPECL Multiplexer	1	0 - 2500	2	LVDS, LVPECL	2.5, 3.3	—	24
853S058i	8:1 Differential-to-3.3V or 2.5V LVPECL/ ECL Clock Multiplexer	1	0 - 2500	8	LVDS, LVPECL, SSTL	2.5, 3.3	—	75
853S057i	4:1, Differential-To-3.3V, 2.5V LVPECL/ ECL Clock Multiplexer	1	0-3000	4	CML,LVDS,LVPECL,SSTL	2.5, 3.3	—	73
85356i	2:1 Differential-to-3.3V Dual LVPECL/ ECL Clock Multiplexer	2	0 - 900	4	HCSL, HSTL, LVDS, LVPECL, SSTL	3.3	150	—
853S54i	Dual 2:1, 1:2 Differential-to-LVPECL/ECL Multiplexer	3	0 - 2500	3	LVDS, LVPECL	2.5, 3.3	—	35
8S89834i	Low Skew, 2-to-4 LVCMOS/LVTTL-to-LVPECL/ECL Clock Multiplexer	4	0 - 1000	2	LVCMOS	2.5, 3.3	30	120
8SLVP1204i	2:4, LVPECL Output Fanout Buffer	4	0 - 2000	2	CML, LVDS, LVPECL	2.5, 3.3	64	32
8T33FS314i	Low Skew, 1-to-4 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	4	0 - 2700	2	LVPECL, ECL, HSTL	2.5, 3.3	50	—
853S014i	Low Skew, 1-to-5 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	5	0 - 2000	2	CML, LVDS, LVPECL, SSTL	2.5, 3.3	55	100
853S310i	Low Skew, 1-to-8 Differential-to-3.3V LVPECL/ECL Fanout Buffer	8	0 - 2000	2	CML, LVDS, LVPECL, SSTL	3.3	40	140
8SLVP1208i	2:8, LVPECL Output Fanout Buffer	8	0 - 2000	2	CML, LVDS, LVPECL	2.5, 3.3	64	31.1
853S111Bi	Low Skew, 1-to-10 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer	10	0 - 2500	2	LVDS, LVPECL, SSTL	2.5, 3.3	50	30
8SLVP1212i	2:12, 3.3V, 2.5V LVPECL Fanout Buffer	12	0 - 2000	2	CML, LVDS, LVPECL	2.5, 3.3	15	45
8T33FS6222	Low Voltage, 1:15 Differential PECL Clock Divider and Fanout Buffer	15	0 - 750	2	PECL	3.3, 2.5	31.25	—

HCSL Multiplexers





9DMV0141 - 2:1 1.8 V PCIe Gen1/2/3 Clock Multiplexer w/Zo=100 W

- One low-power (LP) HCSL DIF pair integrated terminations
- Suitable for PCIe Gen1/2/3 systems
- Output can be easily coupled to LVDS, LVPECL and CML, see AN-891
- < 100 fs RMS additive phase jitter for PCIe Gen3
- 15 mW (typ) power consumption
- Space-saving 3 x 3 mm 16-VFQFPN package; minimal board space

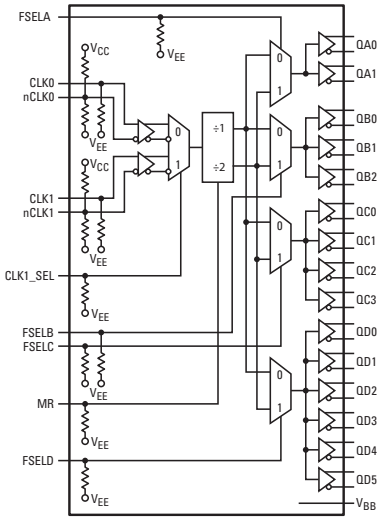
8T39S10i - Crystal or Differential to Differential Clock Fanout Buffer

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal oscillator interface
- Crystal input frequency range: 10 MHz to 40 MHz
- Additive RMS phase jitter: 153 fs (typical)
- 7 x 7 mm 48-VFQFN package

Product ID	Product Title	Outputs (#)	Frequency Range (MHz)	Inputs (#)	Input Type	Supply, Output Voltage (V)	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
5V41068A	2:1 PCIe Gen 1/2/3 Clock Multiplexer	1	0 - 200	2	HCSL	3.3	4500	100
831752i	Clock Switch for ATCA/AMC and PCIe Applications	1	0 - 500	2	HCSL, LVDS, LVPECL	2.5, 3.3	—	300
831721i	2:1 Differential Clock/Data Multiplexer	1	0-700	2	HCSL, LVDS, HSTL, LVPECL	3.3	—	—
831742i	4:2 Differential Clock/Data Multiplexer	2	0 - 700	4	HCSL, LVDS, LVPECL	3.3	15	—
5V41067A	2:4 PCIe Gen 1/2/3 Clock Multiplexer	4	0 - 200	2	HCSL	3.3	50	100
831724i	2:4 HCSL PCIe Clock Buffer	4	0 - 700	2	LVPECL, LVDS, HSTL, SSTL, HCSL	3.3	175	357
8T39S10i	Crystal or Differential to Differential Clock Fanout Buffer	11	0 - 500	3	Crystal, HCSL, LVDS, LVPECL	3.3, 2.5	32	153
9DMU0141	2:1 1.5V PCIe Gen1/2/3 Clock Multiplexer w/Zo=100 Ω	1	1-167	2	HCSL	1.5	—	365
9DMV0141	2:1 1.8V PCIe Gen1/2/3 Clock Multiplexer w/Zo=100 Ω	1	1-200	2	HCSL	1.8	—	284
9DMU0441	2:4 1.5V PCIe Gen1/2/3 Clock Multiplexer w/Zo=100 Ω	4	1-167	2	HCSL	1.5	50	365
9DMV0441	2:4 1.8V PCIe Gen1/2/3 Clock Multiplexer w/Zo=100 Ω	4	1-200	2	HCSL	1.8	50	284
8T39S11	Crystal or Differential to Differential Clock Fanout Buffer	10	0 - 2000	3	Xtal, LVPECL, LVDS, HCSL, HSTL, LVCMOS	2.5, 3.3	35	26

CLOCK DIVIDERS provide an output clock signal that is a divided frequency of the input. They can also be used to provide signal buffering and make multiple copies of the output frequency. Clock divider devices, when used in divide-by-1 mode, can also function as a fanout buffer.

Clock Dividers

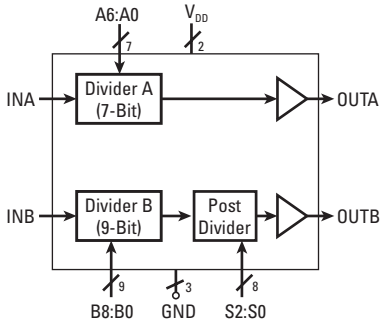


8T33FS6222 - Low Voltage, 1:15 Differential PECL Clock Divider and Fanout Buffer

- 15 differential PECL outputs on 4 separate banks
- Selectable /1 or /2 frequency divider
- Operation to 2 GHz
- 2.5 V or 3.3 V supply
- 10 x 10 mm 52-TQFP package

674-01 - Dual-channel LVCMOS Clock Divider

- General purpose programmable divider
- Supports 673 PLL Building Block
- User determines the divide by setting input pins
- Pull-ups on all select inputs
- Operating voltage of 3.3 V or 5 V
- 6.2 x 10.0 mm 28-SSOP package



Product ID	Product Title	Outputs (#)	Output Type	Frequency Range (MHz)	Input Type	Supply, Output Voltage (V)	Divider Value	Output Skew (ps)	Additive Phase Jitter Typ RMS (fs)
87001I-01	LVCMOS/LVTTL Clock Divider	1	LVCMOS	0 - 250	LVCMOS	2.5, 3.3	1, 2, 3, 4, 5, 6, 8, 16	—	—
8S89874i	1:2 Differential-to-LVPECL Buffer/Divider	2	LVPECL, ECL	0 - 2000, 0 - 1250, 0 - 625, 0 - 312.5, 0 - 156.25	CML, LVDS, LVPECL	2.5, 3.3	1, 2, 4, 8, 16	15	200
8S89875i	Differential-to-LVDS Buffer/ Divider with InternalTermination	2	LVDS	0 - 2500, 0 - 1250, 0 - 625, 0 - 312.5, 0 - 156.25	CML, LVDS, LVPECL	2.5	1, 2, 4, 8, 16	15	—
8V74S4622	Clock Fanout Buffer/ Frequency Divider	2	LVDS	0 - 2000	LVDS, LVPECL	3.3	2, 4, 5, 8	22	114
8S89876i	Differential-to-LVDS Buffer/ Divider with Internal Termination	2	LVDS	0 - 2000	CML, LVDS, LVPECL	3.3	1, 2, 4, 8, 16	25	70
558-01	PECL/CMOS to CMOS Clock Driver	2	LVCMOS	0 - 156	LVCMOS	3.3	2, 4, 6, 8, 12, 16		—
542	Clock Divider	2	LVCMOS	0 - 200, 0 - 235	LVCMOS	5	1, 2, 4, 5, 6, 7, 8, 10		—
8P73S674i	Differential-to-1.8V LVPECL Clock Divider and Fanout Buffer	4	LVPECL	0 - 1000, 0 - 500, 0 - 250, 0 - 125	LVDS, LVPECL	1.8	1, 2, 4, 8	100	60
8V79S674	Differential-to-3.3V, 2.5V LVPECL Clock Divider and Fanout Buffer	4	LVPECL	0 - 1000, 0 - 500, 0 - 250, 0 - 125	LVDS, LVPECL	2.5, 3.3	1, 2, 4, 8	22	60
674-01	Dual-channel LVCMOS Clock Divider	4	LVCMOS	0 - 250	LVCMOS, LVPECL	3.3, 5	1, 2, 3, 4		—
8T73S208i	Differential LVPECL Clock Divider and Fanout Buffer	8	LVPECL	0 - 1000	LVDS, LVPECL, CML	2.5, 3.3	÷1, ÷2, ÷4, ÷8	15	172
8T79S818I-08	1-to-8 Differential to Universal Output Clock Divider/Fanout Buffer	8	Selectable LVDS, LVPECL	0 - 1500	LVDS, LVPECL, CML	2.375 V to 3.465 V	÷1 through ÷6, ÷8	80	—
8T74S208i	Differential LVDS Clock Divider and Fanout Buffer	8	LVDS	0 - 1000	LVDS, LVPECL, CML	2.5	÷1, ÷2, ÷4, ÷8	45	96
8T33FS6222	Low Voltage, 1:15 Differential PECL Clock Divider and Fanout Buffer	15	LVPECL	0 - 750	PECL	3.3, 2.5	1, 2	31.25	—
87016i	Low Skew, 1-to-16 LVCMOS/ LVTTL Clock Generator	16	LVCMOS	0 - 250	LVPECL, LVDS, LVHSTL, SSTL, HCSL	1.8, 2.5, 3.3	÷1, ÷2	170	—

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